Cantilever based sensors for surface stress measurements

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Cantilever-based Sensors for Surface Stress Measurements

Ph.D. Thesis

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Preface

This thesis is submitted as a partial fulfillment of the requirements to obtain the Ph.D. degree at the Technical University of Denmark (DTU). The work has been carried out at the Department of Micro and Nanotechnology (MIC) at DTU from August 1, 2000 to August 31, 2003.

This Ph.D. project has been part of the Bioprobe project and has been supervised by project leader Anja Boisen. The work was financed by DTU within the Electronics and Communications programme.

Acknowledgements

As always with works of this kind a lot of people contributed by sharing some of their knowledge and some of their time. Firstly, I would like to thank Anja for encouraging me to do this Ph.D. project, I can't imagine I would have got a more interesting job anywhere else. I feel like I have had several supervisors I need to thank. Erik Thomsen was effectively my supervisor during Anja's leave, and Jacob Thaysen, who was working in the group when I started, was certainly an extra supervisor during the first year of my project. The rest of the Bioprobe group deserve acknowledgement for their interest in my work and for creating a pleasant working atmosphere. I would like to thank Christian B. Nielsen for help and advice about the finite element simulations and for instructive discussions about the mechanics of my system in general. I also need to thank Zachary Davis for doing the finite element simulations, supplying me with nice figures of which you can never get enough. I would like to thank Steen Eriksen for doing the immobilisation tests on the polysilicon sensor. For the testing of the SOI chip I would like to thank Rodolphe Marie for the packaging of the chips and for doing the tests in the biochemical setup, and, once again, I would like to thank Christian B. Nielsen for assisting with the electrolytic cell when measuring leak currents. Most of the cleanroom work on SU-8 has been done by Montserrat Calleja, and I would like to thank her for our nice collaboration during the last 18 months. Additionally, Alicia Johansson needs acknowledgement for her work with the processing of SU-8; she has during her Master's project made an enormous amount of tests, which have been of great value for the rest of the

SU-8 work in the group. I would like to thank Torben Lisby at Delta for the wire bonding tests done on the SU-8 chips and, before leaving MIC, helping me with my SIMS measurements. I would like to thank the lab technicians for the professional and yet relaxed atmosphere in the cleanroom, especially I need to mention Lis Nielsen and Pernille H. Nielsen who taught me how to write a process sequence that can actually be interpreted by other people. For input on the processing of titanium silicide I would like to thank Thomas Clausen. I would like to thank Ole Hansen for help on just too many subjects to be mentioned here, and if I tried it would just resemble the table of contents too much. I would like to thank Frank Rasmussen for discussions ranging from mortgage to PECVD techniques. Also I would like to thank Christian, Jacob, Jamil, René, Salim and Zach for memorable work on theoretical as well as experimental HL-techniques. I would like to thank my father for always being willing to hear about the project; a more interested listener is hard to find, and I would like to thank my mother and sister for, thank God, never asking me about my work, but instead asking about Kirsten and Charlotte, to whom my last thanks go. After seing months of work being destroyed in the KOH bench, you have been wonderful to come home to.

August 31, 2003

Peter Andreas Rasmussen

Abstract

The work presented in this Ph.D. thesis deals with the development of cantilever surface stress sensors. The aim is to use this sensor as a biochemical sensor; small micrometer sized cantilevers have been shown to be sensitive to the surface stress that is created when molecules adsorb on the surface of the cantilever. The readout technique for measuring the cantilever bending investigated in this work is the deformation of an integrated resistor. This deformation creates a resistance change of the resistor that is a measure of the bending of the cantilever. This readout technique is believed to be useful for making compact devices with many cantilevers for the purpose of measuring several biological species simultaneously. Such a measurement is usually made by inserting the cantilever into the liquid sample. In order to measure specific chemical species, the cantilever needs to be coated with a layer that binds these with a high degree of selectivity to other chemical components in the sample. A device like this can be thought of as a candidate for point-of-care analysis, which is diagnostic testing taking place at, for example, a physician's office, directly where the sample is taken.

A cantilever sensor, with polysilicon as the strain gauge material and titanium silicide as the on-chip wiring, was developed. Both resistors and wiring were encapsulated in LPCVD silicon nitride to make efficient protection of the electrical on-chip circuit against the buffer liquid that contains the analytes in biochemical measurements.

To gain in resolution a new sensor was designed and partially realised, which features single crystalline silicon strain gauges. Single crystalline silicon makes more sensitive strain gauges than polysilicon and, at the same time, the electrical noise from a single crystalline silicon resistor is much lower than that of a polysilicon resistor. The principle resolution limit for a device made by the design described here should be close to the resolution limit set by thermal mechanical noise.

A device including an array of cantilevers made entirely in the polymer SU-8 was presented. The integrated strain gauge is made of gold. This presents a potentially cheap device with a processing time much lower than that of comparable silicon devices.

Resumé

Denne Ph.D.-afhandling omhandler udviklingen af en sensor til måling af den mekaniske spænding, der induceres på overfladen af en bjælke ved adsorption af kemiske komponenter på overfladen. Det har vist sig, at bjælker i mikrometerstørrelsen kan bøjes af disse kraftpåvirkninger og dermed kan bruges til at detektere de adsorberede komponenter. Udlæsningen af bjælkens bøjning foregår ved hjælp af en indbygget 'strain gauge'(elektrisk modstand), hvis modstand ændres, når den deformeres ved bjælkens udbøjning. Denne udlæsningsmetode vil kunne bruges i kompakte apparater, der indeholder mange bjælker ved siden af hinanden, med det formål at kunne måle flere kemiske komponenter samtidigt. En sådan måling foregår typisk ved, at bjælken anbringes i den væskeprøve, der ønskes undersøgt. For at måle et specifikt stof kræves det, at bjælken dækkes med en overfladebelægning, der binder dette stof med stor selektivitet i forhold til andre kemiske komponenter i prøven. Et apparat som dette kan tænkes anvendt som et såkaldt 'point-of-care' analyseinstrument, der for eksempel kan anvendes hos den praktiserende læge, hvor prøver til analyse i stort omfang udtages.

En bjælkesensor med polysilicium strain gauge og titaniumsilicid ledebaner blev udviklet. Siliciummodstandene og ledebanerne blev indkapslet i LPCVD siliciumnitrid for at beskytte det elektriske kredløb på komponenten mod den væske, som indeholder de biologiske komponenter.

For at forbedre opløsningen blev en ny bjælkesensor designet og delvist virkeliggjort, hvor strain gaugen blev fremstillet af enkeltkrystallinsk silicium. En strain gauge udført i enkeltkrystallinsk silicium er mere følsom og samtidig er den elektriske støj mindre, end hvis den var udført i polykrystallinsk silicium. I princippet vil en komponent lavet på denne måde kunne måle mekaniske spændinger med en opløsning, der er tæt på den teoretiske grænse for opløsningen bestemt af den termisk inducerede mekaniske støj.

En komponent blev præsenteret, hvor en række bjælker blev fremstillet i det fotofølsomme plastmateriale SU-8, og hvor den indbyggede strain gauge var lavet af guld. Denne komponent kan fremstilles ved en hurtigere og enklere procesfølge end tilsvarende siliciumkomponenter og bliver dermed en potentielt billigere komponent at fremstille.

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Chapter 1

Introduction

1.1 Cantilever sensors

The use of cantilevers to measure forces dates back to the invention of the atomic force microscope (AFM) in 1986 by Binnig *et al.*[1]. The AFM basically consists of a soft plate or cantilever that is brought in contact with a sample. Figure 1.1 shows a schematic presentation of a generic AFM probe with a tip included at its apex to improve horizontal resolution. The bending of the cantilever is monitored and in this way the AFM plots the interatomic interaction between the tip of the AFM probe and the surface of the sample, which is usually interpreted as a contour plot of the sample. The AFM sensor can scan a sample much like the

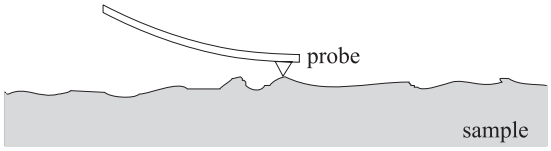


Figure 1.1: Schematic presentation of an AFM probe. Typically the sample is placed on a piezoelectric tube and scanned under the AFM probe.

scanning tunnelling microscope (STM) invented in 1982[2], but contrary to the STM that can only picture conducting samples, the AFM with its mechanical interaction can picture both non-conducting and conducting samples. The first AFM probe consisted of a thin metal plate and an STM placed above the plate measuring the bending. The STM readout tip was a limiting factor for the first AFM as it exerted a high force on the cantilever and a low force is desirable in order not to damage the pictured sample[3].

Soon after the invention of the AFM micromachining techniques[4] were used to make cantilevers in materials widely used and investigated in the microelectronics industry like silicon, silicon oxide and silicon nitride[5, 6], making it possible

to produce small cantilevers with high resonant frequencies - which for example make them less susceptible to external mechanical noise - at the same time as having low spring constants.

At the same time new optical readout mechanisms using optical interferometry were developed[7] that do not exert any force on the cantilever. Today the most frequently used readout technique is the laser beam leverage technique presented by Meyer and Amer in 1988[8] where a laser beam is focused on the back of the cantilever and the angle of the deflected laser beam gives the deflection angle of the cantilever as sketched in figure 1.2.

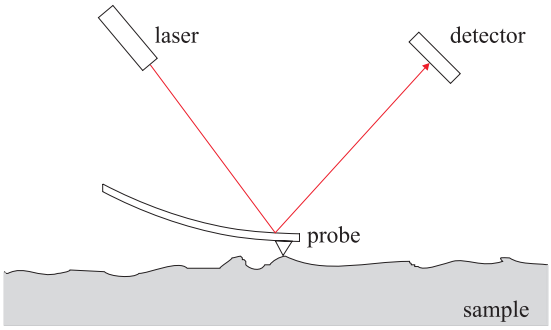


Figure 1.2: Schematic presentation of an AFM probe with the laser leverage readout technique.

In 1991 Tortonese *et al.* presented the first AFM cantilever with piezoresistive readout[9]. The deformation of a silicon resistor in the cantilever changes its resistance, and this resistance change is the measure of the bending of the cantilever. Other readout mechanisms have been reported[10, 11] but the optical leverage technique and the piezoresistive readout are by far the most widely used readout mechanisms.

AFM cantilevers with piezoresistive readout are commercially available from Veeco Metrology Group[12](Park Scientific Instruments).

Among groups at universities publishing work on the development of cantilevers with piezoresistive readout can be mentioned Quate's[9, 13, 14] and Kenny's[15, 16, 17] groups at Stanford, Rangelow's group at the University of Kassel[18, 19, 20], Baltes's group at ETH Zürich[21, 22], and the Bioprobe project at the Technical University of Denmark[23, 24, 25].

AFMs are routinely used for picturing solid surfaces and the deflection resolution is around 1 Å so atomic resolution is possible[26]. The AFM has proved its

versatility by being applied to measure a wide variety of solid state matters from atomically flat graphite[5] to biological samples like DNA strands [27, 28, 29].

The cantilever sensors developed for AFM have been applied and shown capable of measuring other physical quantities than the force interactions from the AFM measurements. These include the measurement of temperature changes causing the cantilever to bend because of the bimorph effect as reported by Gimzewski *et al.*[30], the measurement of mass changes obtained through the change in resonant frequency of a vibrating cantilever caused by the adsorbed mass as reported by Thundat *et al.*[31], and surface stress changes typically measured via the bending as described in the review by Raiteri *et al.*[32]. The measurement of the latter two physical quantities has been put to use in a broad field that has developed since the mid nineties and can be described under the headline:

1.2 Chemical and biochemical cantilever based sensors

Changes in surface stress due to adsorption (of molecules) on cantilevers was reported by Raiteri *et al.*[33] and Chen *et al.*[34] in 1995 and Butt[35] and O'Shea *et al.*[36] in 1996, and this showed the potential use of micro cantilevers developed for AFM as biochemical sensors. Major advantages of the direct detection on the cantilever are:

- *In situ*/real time measurements as surface stress develops.
- The possibility of label free detection so that the molecules to be detected do not need pre-treatments. The requirement for detection is the ability to make a coating on the cantilever that reacts specifically with the analyte.

The use of micromachined cantilevers as chemical sensors can be differentiated into two branches:

- *Dynamic* measurements which refer to measurements where mass and surface stress changes due to adsorption are measured via a change in the resonant frequency of the cantilever.
- *Static* measurements which refer to measurements of static cantilever deflection.

In the following, if nothing else is stated, the readout technique is the optical leverage technique.

1.2.1 Dynamic measurements

The measurements by Chen *et al.*[34] were made on resonating cantilevers and showed resonant frequency changes caused both by added mass and by a change in spring constant during adsorption.

The use of cantilevers as gas sensors has been investigated by several groups. Combinations of static and dynamic measurements have been used to distinguish the effects of added mass from the effect of the change in spring constant[37], and arrays of cantilevers have been applied in order to measure several gases simultaneously as well as supplying the possibility to compensate for unspecific adsorption by subtracting signals from reference cantilevers[38, 39].

Dynamic adsorption measurements are usually done in gaseous environments. In liquids the damping is higher and thus the frequency resolution is lower.

1.2.2 Static measurements

In liquid systems as met in most micro total analysis systems(μTAS)[40], where buffers are used to sustain the biochemical species, the static deflection method is commonly used.

Adsorption measurements causing a cantilever bending have been reported with many biological systems. Examples are the detection of the self-assembly of alkanethiols[41] and the detection of the binding of antibody[42, 43].

More recently the detection of hybridisation of DNA has been reported[44, 45, 46]. Fritz *et al.* reported that the hybridisation process gave a surface stress signal of a few mN/m[44].

On cantilever platforms with piezoresistive readout the detection of alcohol in water[47] and the detection of the immobilisation of single stranded DNA has been reported[48, 49].

The application of static deflection measurements is not exclusively used in liquids, and the detection of alcohol vapors absorbed on polymer coated cantilevers has been reported by Baller *et al.*[50] using optical readout and Jensenius *et al.*[51] using piezoresistive readout. As a commercial example Hygrometrix[52] produces a humidity sensor with a polymer coated cantilever and piezoresistive readout.

The general trend for the biochemical sensors has been toward the integration of many cantilevers in arrays to facilitate simultaneous measurements of many

biochemical species, and also the importance of using reference cantilevers to subtract unspecific signals is stressed in several articles[38, 44, 46, 48, 43, 53].

1.3 The Bioprobe project

The cantilever activities that preceded the Bioprobe project at the Technical University of Denmark[1] was the work on AFM cantilevers started by Boisen in 1994[54] and since 1997 the focus has been on developing cantilevers with integrated piezoresistive readout[55]. In 1999 the Bioprobe project was started with the goal of developing cantilever sensors with integrated readout for the use as biochemical sensors. The conviction is that the integrated readout scheme using piezoresistors has some advantages when compared to the more frequently used optical leverage detection method:

- The readout system is much more compact which facilitates the use in large arrays.

- The readout scheme is not affected by the optical properties of the liquids in the system *e.g.* whether the liquid is opaque or the refractive index changes during measurements.

The use of piezoresistive readout, however, introduces some technological difficulties. For one thing, part of the electrical measurement circuit, *i.e.* the piezoresistor, has to be put into for example biological buffers containing salts and therefore needs shielding. Additionally, the piezoresistor introduces electrical noise in the measurement system that often exceeds the noise from pure thermal mechanical vibrations of the cantilever[56, 57].

1.3.1 Overview of thesis

There are two main goals for this project. One major goal is to make cantilever sensors with piezoresistive readout that are optimised for measuring surface stress in biochemical applications. Most such measurements will take place in liquids, and since the Bioprobe project uses the integrated readout scheme, the sensors will have on-chip electrical wiring and resistors. As a consequence of this, the other major goal is to make a cantilever chip that can operate in liquids, and thus includes a protection scheme for wiring and resistors that offers a good diffusion barrier as well as good electrical insulation. Three different sensors have been realised

- one with polysilicon resistors and titanium silicide wiring

[1] At the Department of Micro and Nanotechnology (MIC), http://www.mic.dtu.dk

- one with single crystalline silicon resistors encapsulated in LPCVD silicon nitride

- and one with an array of cantilevers in polymer with gold strain gauges

each of them requiring their own theoretical treatment for optimising the sensitivity.

This thesis does *not* focus on the practical application of the cantilever sensor in biochemical measurements. The noise levels, the sensitivities and the derived resolutions obtainable only refer to the inherent noise in the cantilever sensor itself. For considerations on noise and sensitivities in a full biochemical measurement setup including lock-in amplifier and mechanical noise from *e.g.* pumps in the liquid circuit, and for the investigation of specific biochemical applications, I would like to refer to the work of Rodolphe Marie, who has been doing his Ph.D. in the Bioprobe project simultaneously with the work described in the present thesis.

Outline of chapters

Chapter 2 gives a general description of the cantilever sensor developed in the Bioprobe project. This is followed by the suggestion for a new wiring and encapsulation scheme for the Bioprobe chip.

Chapter 3 deals with the mechanics of cantilevers. The design of the cantilever chip with piezoresistors is presented. The strain in the piezoresistor as a function of loading is investigated and theoretical expressions for sensitivity and resolution are derived.

Chapter 4 describes tests with producing, contacting and encapsulating titanium silicide wiring and high doped silicon wiring.

Chapter 5 describes the design, fabrication and testing of cantilever sensors with polysilicon piezoresistors.

Chapter 6 describes the first generation of a new surface stress sensor developed on an silicon on insulator (SOI) substrate. In this design the piezoresistors are made of single crystalline silicon to improve the sensitivity and resolution obtainable with the sensor.

Chapter 7 describes the development of a new cantilever platform made in the epoxy-based photoresist SU-8 with integrated metal strain gauge readout. The platform includes an array of cantilevers integrated in a micro liquid system.

Chapter 8 gives the main conclusions of the work presented in this thesis.

Appendix A lists the conference and journal papers that have been made during the course of this project.

Appendix B gives the detailed process sequence for the 1st generation polysilicon sensor.

Appendix C includes the mask set for the 2nd generation polysilicon sensor.

Appendix D gives the detailed process sequences for the 1st generation polysilicon sensor.

Appendix E gives the detailed process sequence for the 3rd generation polysilicon sensor.

Appendix F gives the detailed process sequence for different high doped silicon wiring schemes.

Appendix G gives the detailed process sequence for the SOI sensor.

Chapter 2

Design of the Bioprobe cantilever sensor

Before going into detail with the theory and the preliminary processing tests, which are the topics of the next two chapters, a general description of the cantilever sensor is needed. The piezoresistive readout and the design and layout of the on-chip resistors are described in chapter 3. As mentioned in the introduction a sensor which works in liquid is required. For this the silicon piezoresistor is encapsulated in low pressure chemical vapor deposition (LPCVD) silicon nitride, which both acts as a good electrical insulator and is considered to be a good diffusion barrier. The cantilever is sketched in figure 2.1. Chromium/gold has

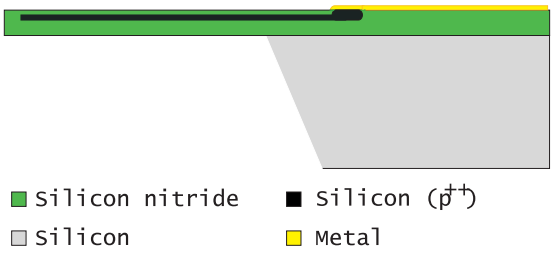


Figure 2.1: Schematic drawing of the Bioprobe cantilever sensor. It consists of a piezoresistive polysilicon resistor encapsulated in silicon nitride.

been the preferred choice for the on-chip wiring that contacts the piezoresistor.

In this design the resistor is protected but a coating is needed to protect the wires on the chip. One solution used extensively in the Bioprobe group has been to coat the wires with either a vacuum wax[47, 58, 49] or a UV-glue, as shown in figure 2.2(a). This is a single chip coating process made by hand and it is time consuming and obviously has an alignment precision much inferior to that of lithography. In a more recent approach that can be used on the chips as a wafer

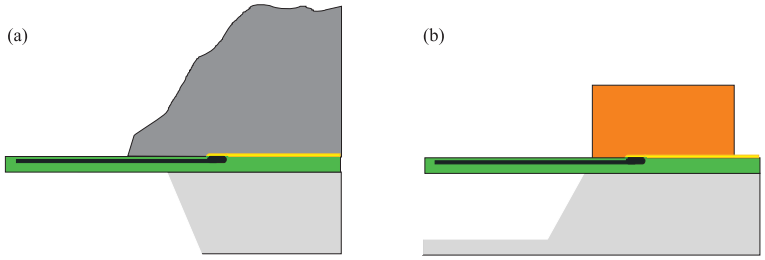


Figure 2.2: Schematic view of coating with glue or wax in figure (a) and with SU-8 in figure (b).

scale protection of the wiring, a thick layer of the photoresist SU-8[59] covers the metal wires[57]. The SU-8 is spun and patterned to make the top part of a flow channel at the same time as protecting the wires from the liquid, as sketched in figure 2.2(b). This is done after the cantilevers have been released by etching the bulk silicon under the cantilever, and the method can only be used on chips where the cantilevers are released from the front of the wafer, so that it is possible to spin the resist on the wafer. One problem with this coating has been to make the SU-8 adhere so well to the surface that liquid does not penetrate under the SU-8 causing a short circuit or an electrochemical etch of the metal wiring.

2.1 New wiring scheme

To solve the shortcomings of the above mentioned coating methods, it will be tried in this work to make the on-chip wiring compatible with the LPCVD silicon nitride coating process so that resistors and wiring are coated in the same process step. This excludes the use of commonly used metal wirings such as gold and aluminum, as they are not stable at the high temperatures in the LPCVD process of around 800°C. Lower temperature (300°C) plasma enhanced chemical vapor deposition (PECVD) coatings are available but they do not have the excellent step coverage of the LPCVD process nor do they have as high a chemical resistance as LPCVD silicon nitride.

A suitable solution is to make the wiring of highly doped silicon. The advantage of this method is that there are no compatibility issues. The disadvantage is that silicon has a much higher resistivity than the usual metal wiring, and thus introduces a larger series resistance to the piezoresistors, which in turn will decrease the sensitivity of the sensor.

Titanium silicide is chosen, as the candidate for the wiring, as it can stand the high-temperature processing and has a low resistivity. Titanium and silicon heated to about 800°C will form a titanium disilicide, $TiSi_2$, with a resistivity of

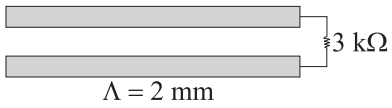


Figure 2.3: Schematic view of wiring and resistor. These are typical dimensions and values for a piezoresistor and its wiring for the cantilever sensors used in the Bioprobe project. The wires have a length and width of Λ=2 mm and w=100 µm. The series resistance for the wiring, with a resistivity of ϱ and a thickness of t, is $R_{wiring} = \varrho\frac{2\Lambda}{tw}$.

	ϱ [Ω·cm]	R_{wiring} [Ω]	R_{wiring}/R_{total}
Au	$2.2{\cdot}10^{-6}$	4.4	1.5 ‰
Si	$5{\cdot}10^{-3}$	2000	40 %
$TiSi_2$	$20{\cdot}10^{-6}$	40	1.3 %

Table 2.1: Resistances for different wirings. For the gold and silicide wiring the thickness is 0.2 µm and for the silicon a thickness of 1 µm is used. The silicon is highly doped polysilicon. The last column gives the relative series resistance of the wiring in series with a 3 kΩ piezoresistor.

20 µΩ·cm[60]. Titanium silicide is stable up to 1500°C[61] and is therefore easily compatible with the temperatures in the LPCVD process. Since, moreover, it has a resistivity that is approximately two orders of magnitude lower than that of the silicon, it will give a lower series resistance.

As an example to show what is gained by using titanium silicide, a typical chip used in the Bioprobe project has on-chip leads with a length and width of 2 mm and 100 µm, and the piezoresistor has a resistance of 3 kΩ. This example is outlined in figure 2.3. For this chip the series resistances is calculated for gold, silicon and titanium silicide wiring and the results are shown in table 2.1. To make a realistic comparison, the thickness of the gold and the silicide wiring is 0.2 µm and for the polysilicon wiring the thickness is 1 µm. It is seen that even though the series resistance of the silicide wiring is ten times higher than that for the gold wiring, the series resistance is still only about 1 % and can to a good approximation be considered negligible. The silicon wiring has a resistance comparable to that of the piezoresistor, almost reducing the sensitivity by a factor of 2.

2.2 Summary

Titanium silicide was introduced as a wiring material that fulfils the requirements of low resistivity and compatibility with the LPCVD silicon nitride coating process that is already used to encapsulate the piezoresistors.

The processing and encapsulation of the wiring will be pursued in chapter 4 and the integration of the new wiring scheme is described in chapter 5.

Chapter 3

Theory

In this chapter the mechanical theory of bending cantilevers will be presented. The emphasis will be on the analytical expressions needed for designing cantilevers for some specific applications, meaning that this is not a thorough treatment of the mechanics of beams and plates. As will be specified in the following, the analytical models will give precise solutions in specific limits of the parameter space, but cannot be expected to give exact solutions if used generally. The two different applications of the cantilevers dealt with here will be the original use of micro cantilevers as force or deflection sensors, known from AFM, and then the use of micro cantilevers in biosensing where isotropic surface stresses are encountered. The objective is to obtain design parameters for the cantilever based sensor with piezoresistive readout.

3.1 Cantilevers

Two of the important characteristics of cantilevers are the resonant frequency and the spring constant. In the following the spring constant and the resonant frequency will be derived for a rectangular cantilever with length L, width w and thickness t.

The deflection u of a cantilever is given by[62]

$$\frac{d^2u}{dx^2} = -\frac{M}{EI} \tag{3.1-1}$$

where M is the bending moment, E is Young's modulus, and I is the cross sectional area moment of inertia. I is given by $\frac{wt^3}{12}$ for the rectangular cantilever. The spring constant k assigned to a cantilever is found from Hooke's law

$$F = -ku(L) \tag{3.1-2}$$

where F is a force acting on the cantilever as sketched in figure 3.1. For this force

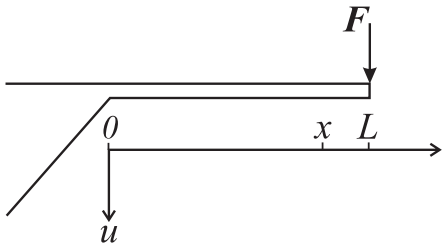


Figure 3.1: Force acting on a cantilever.

working on the cantilever, the bending moment $M = -F(L - x)$ and equation 3.1-1 is solved with the clamped beam boundary conditions

$$\begin{aligned} u(0) &= 0 \\ \left.\frac{du}{dx}\right|_{x=0} &= 0 \end{aligned} \tag{3.1-3}$$

The solution is

$$u(x) = \frac{FLx^2}{2EI}(1 - \frac{x}{3L}) \tag{3.1-4}$$

and the bending at the apex is then

$$u(L) = \frac{L^3}{3EI}F \tag{3.1-5}$$

and hence the spring constant

$$k = \frac{3EI}{L^3} = \frac{Ewt^3}{4L^3} \tag{3.1-6}$$

The resonant frequency is found by solving the beam equation, balancing bending and inertial forces, as done by *e.g.* Sarid[63]:

$$EI\frac{\partial^4 u}{\partial x^4} + \rho A\frac{\partial^2 u}{\partial t^2} = 0 \tag{3.1-7}$$

where ρ is the density and A is the cross sectional area of the beam. The beam equation is solved with the boundary conditions of a clamped beam at x=0 and a free end at x=L:

$$\begin{aligned} u(0) &= 0 \text{ and } \left.\frac{\partial u}{\partial x}\right|_{x=0} = 0 \\ \left.\frac{\partial^2 u}{\partial x^2}\right|_{x=L} &= 0 \text{ and } \left.\frac{\partial^3 u}{\partial x^3}\right|_{x=L} = 0 \end{aligned} \tag{3.1-8}$$

This equation has the solution

$$u(x,t) = u(x)\cos(\omega_n t + \theta) \tag{3.1-9}$$

with the spatial part

$$u(x) = (\sin c_n L + \sinh c_n L)(\cos c_n x - \cosh c_n x) - (\cos c_n L + \cosh c_n L)(\sin c_n x - \sinh c_n x) \tag{3.1-10}$$

where

$$c_n^4 = \frac{\omega_n^2 \rho A}{EI} \tag{3.1-11}$$

relates the wavenumber c_n to the resonant frequency ω_n. Applying the boundary conditions yields the characteristic equation for the allowed wavenumbers

$$\cos(c_n L)\cosh(c_n L) + 1 = 0 \tag{3.1-12}$$

which solves for

$$c_n L = 1.875, 4.694, 7.855, \ \ldots \ \ n = 1, 2, 3, \ldots \tag{3.1-13}$$

where the solutions represent different resonant modes with $n = 1$ being the fundamental mode. The resonant frequency f is then

$$f_n = \frac{c_n^2}{2\pi}\sqrt{\frac{EI}{\rho A}} \tag{3.1-14}$$

Substituting for $I = \frac{wt^3}{12}$ and $A = wt$

$$f_n = \frac{c_n^2}{4\sqrt{3}\pi}\sqrt{\frac{Et^2}{\rho}} \tag{3.1-15}$$

or

$$f_n = \frac{(c_n L)^2}{2\sqrt{3}\pi}\sqrt{\frac{k}{m}} \tag{3.1-16}$$

where m is the mass $\rho L w t$ of the cantilever. Then the resonant frequency for the fundamental mode can be written

$$f_{res} = 0.1615\sqrt{\frac{E}{\rho}}\frac{t}{L^2} = 0.3231\sqrt{\frac{k}{m}} \tag{3.1-17}$$

For a cantilever made of silicon with a Young's modulus of 170 GPa, a length of $L = 150$ μm, and a thickness of $t = 0.5$ μm

$$k = 0.079 \text{ N/m and } f_{res} = 31 \text{ kHz}.$$

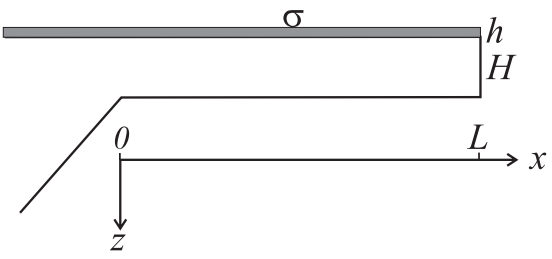


Figure 3.2: Stress σ in thin film of thickness h on top of cantilever. The surface stress σ_s is introduced as $h\sigma$.

The objective of this work is to measure isotropic in-plane stresses, more specifically surface stresses, and an equivalent spring constant can be found for this case. To illustrate a surface stress, a cantilever consisting of two layers of thickness h and H, with $H \gg h$, is considered. The thin layer has an in-plane stress of σ as outlined in figure 3.2. In this case there is an in-plane force working around the neutral axis of the cantilever, but as in the case with the apex force creating a moment acting around the base of the cantilever, there is still a bending moment being perpendicular to the plane of the drawing. So, with $F = wh\sigma$ and $M = wh\sigma z$, where $z = -H/2$ since $H \gg h$, equation 3.1-1 is solved again, and the deflection is now

$$u(x) = \frac{wHx^2}{4EI}\sigma_s \tag{3.1-18}$$

where the surface stress is introduced as $\sigma_s = h\sigma$. This applies for uniaxial surface stress along the the x-axis, while for the more realistic biaxial stress the Young's modulus is replaced with the biaxial modulus $E/(1-\nu)$, where ν is the Poisson's ratio of the material (see section 3.3). The spring constant for surface stress k_{σ_s} is defined from

$$\sigma_s = k_{\sigma_s} u(L) \tag{3.1-19}$$

and is given by

$$k_{\sigma_s} = \frac{4EI}{(1-\nu)wHL^2} = \frac{EH^2}{(1-\nu)3L^2} \tag{3.1-20}$$

Small surface stresses from *e.g.* hybridisation are on the order of mN/m. For a cantilever made of silicon and with $L = 150$ µm, $w = 50$ µm and $t = 0.5$ µm the spring constant k_{σ_s} is $6.3 \cdot 10^5$ N/m^2. With a surface stress of $\sigma_s = 1$ mN/m the bending is 1.6 nm.

To make a comparison, the bending due to gravity can be found. For a force per unit length of $\frac{dF}{dx} = \rho twg$, where g is the acceleration of gravity, the bending is given by[64]

$$u(L) = \frac{\rho twgL^4}{8EI} = \frac{3\rho gL^4}{2Et^2} \tag{3.1-21}$$

This yields a bending of 4 Å at the apex. So for this example the bending due to (a small) surface stress is only four times larger than that due to gravity.

3.2 Piezoresistor design

As mentioned in the introduction, the focus of this work is to use piezoresistive readout, and this section introduces the resistor design.

3.2.1 Piezoresistivity

A piezoresistive material changes its resistance when it is strained. Most materials will change both cross section and length under load and thus change resistance, but the resistance change of piezoresistive materials is larger than what can be accounted for by the geometrical effects. When geometrical effects are omitted, the relative resistance change for a piezoresistor is written as

$$\frac{\Delta R}{R} = K_L \varepsilon_L + K_T \varepsilon_T \tag{3.2-1}$$

where ε is strain and K is the gauge factor of the material. The subscripts L and T mean longitudinal and transversal with respect to the direction of the current flowing in the resistor, see figure 3.3.

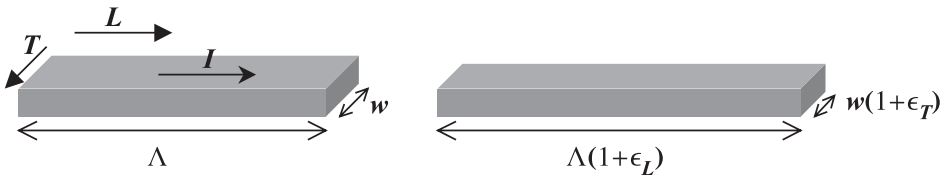


Figure 3.3: The longitudinal direction is along the current lines and the transversal direction is perpendicular to the current lines. The resistor to the right is under tension.

3.2.2 Geometry of piezoresistors

The basic geometry of the piezoresistors used in the Bioprobe project[55, 24] is sketched in figure 3.4 along with the piezoresistor's placement on the cantilever. The resistor can be split into two regions: The 'legs' where the current lines are assumed to run along the x-direction, and the 'top' where the current lines presumably are following the y-direction. From this follows that the strain in the x-direction is considered as the longitudinal strain component in the legs and the transversal strain component in the top. Using equation 3.2-1 on the legs and

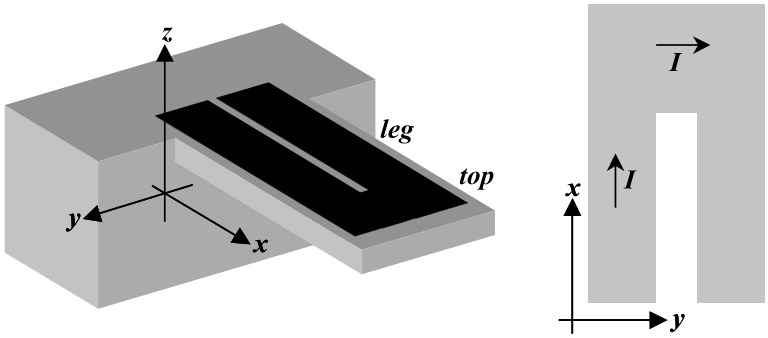


Figure 3.4: Geometry of piezoresistor. To the left is shown the piezoresistor placed on a cantilever. I is the current running through the resistor.

top of the resistor separately, leads to the following relationships

$$\begin{aligned} \frac{\Delta R}{R}\bigg|_{leg} &= K_L\varepsilon_x + K_T\varepsilon_y \\ \frac{\Delta R}{R}\bigg|_{top} &= K_L\varepsilon_y + K_T\varepsilon_x \end{aligned} \tag{3.2-2}$$

The total relative resistance change experienced by the resistor is found by weighing the two contributions by their relative resistances $A = \frac{R_{leg}}{R_{total}}$ and $B = \frac{R_{top}}{R_{total}}$, where R_{leg} is the resistance of the two legs in the resistor

$$\begin{aligned} \frac{\Delta R}{R} &= A\frac{\Delta R}{R}\bigg|_{leg} + B\frac{\Delta R}{R}\bigg|_{top} \\ &= \varepsilon_x(AK_L + BK_T) + \varepsilon_y(AK_T + BK_L) \end{aligned} \tag{3.2-3}$$

A simplifying case could be where the resistance of the top part of the resistor is negligible compared to the total resistance for example because of the design or a high doping concentration so that $A \approx 1$ and $B \approx 0$.

3.3 Different strain regimes

The clamping of cantilevers imposes a restriction on one end of the cantilever beam, but often this restriction is considered negligible - and often justifiably so if the cantilever has a high length to width aspect ratio - and the cantilever is treated as a 'free' bending beam. The term beam is used for a cantilever with high length to width ratio, whereas the term plate will be used for low length to width ratios, where the clamping plays a dominant role for the bending of the cantilever.

The strain in the cantilever for four scenarios will be shown here and applied

to the result from section 3.2.2. The scenarios will include strains caused by a force applied vertically at the apex of the cantilever, which henceforth will be referred to as an 'apex force', and they will include strains caused by an in-plane isotropic stress.

The strain for an elastic isotropic material is given by[62]

$$\begin{aligned} \varepsilon_x &= \frac{1}{E}(\sigma_x - \nu(\sigma_y + \sigma_z)) \\ \varepsilon_y &= \frac{1}{E}(\sigma_y - \nu(\sigma_x + \sigma_z)) \end{aligned} \tag{3.3-1}$$

where σ is the stress, E is Young's modulus, and ν is Poisson's ratio for the material. The stress out of the plane of the cantilever σ_z, see figure 3.4, is zero in all cases. The stress in the x direction will be assumed to be known whether it is in-plane stress or it originates from an apex force.

A: Apex force, beam

Free Poisson contraction is assumed for a beam since $L \gg w$. Free Poisson contraction means that the cantilever is not constraint in the y-direction by the clamping. With this assumption $\sigma_y = 0$ and from equation 3.3-1 it follows

$$\varepsilon_x = \frac{\sigma_x}{E} \tag{3.3-2}$$

$$\varepsilon_y = -\nu\frac{\sigma_x}{E} \tag{3.3-3}$$

For this typical AFM case with a long slender beam, it is seen that the strain component ε_x along the length axis of the cantilever is the dominant part as Poisson's ratio typically will be around 0.25.

B: Apex force, plate

With the plate constriction from $L \sim w$, the cantilever will be considered to be rigidly clamped so that $\varepsilon_y = 0$ and from equation 3.3-1

$$\sigma_y = \nu\sigma_x \tag{3.3-4}$$

$$\varepsilon_x = (1-\nu^2)\frac{\sigma_x}{E} \tag{3.3-5}$$

From the definition above only the strain in the x direction is contributing to the resistance change. $E/(1-\nu^2)$ is the so-called plate modulus.

C: In-plane stress, beam

A uniform in-plane stress, as measured with biosensors, will resolve in $\sigma_x = \sigma_y$. With this constraint we do not get the free Poisson contraction $\varepsilon_y = -\nu\varepsilon_x$, which was found in case A. Rather, the strain in x and y will equal

$$\varepsilon_x = \varepsilon_y = (1-\nu)\frac{\sigma_x}{E} \tag{3.3-6}$$

meaning that the radius of curvature for the cantilever bending is the same in x and y. $E/(1-\nu)$ is referred to as the biaxial modulus.

D: In-plane stress, plate

With the rigid clamping, as described above, $\varepsilon_y = 0$. This gives the same solution as in case B.

A finite element (FEM) analysis using CoventorWare^{TM} of the stress and the strain in a simple cantilever has been carried out in order to check the validity of the above analytical expressions. In figure 3.5 the longitudinal and the transversal strains in a cantilever with an in-plane stress are shown. The modelled cantilever

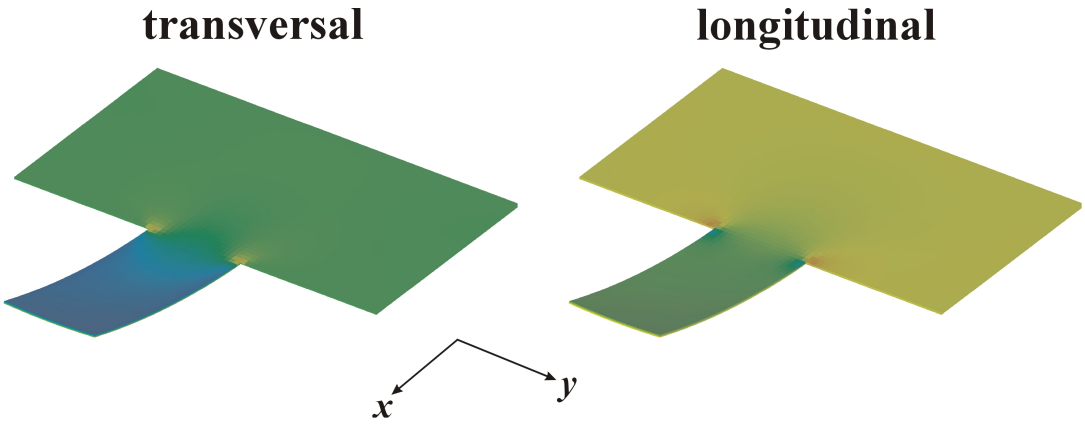


Figure 3.5: Longitudinal(x) and transversal(y) strain in a 1 μm thick cantilever with a 0.1 μm thick gold layer on top. The gold has a uniform in-plane tensile stress. The plots show the strain in the cantilever just below the gold layer. Though the colour scales are different, the strain on the support is zero in both cases. The bending is exaggerated.

is made of polysilicon and has a length, width and thickness of: L=100 μm, w=50 μm and t=1 μm. On top of the cantilever is a 0.1 μm gold layer with a biaxial stress in the xy-plane of 50 MPa. The numerical values for longitudinal and transversal strain and stress are plotted in figure 3.6. The values are taken for the top of the silicon cantilever along the length axis and in the middle of the cantilever. The cantilever is clamped at 0 μm and the apex of the cantilever is at 100

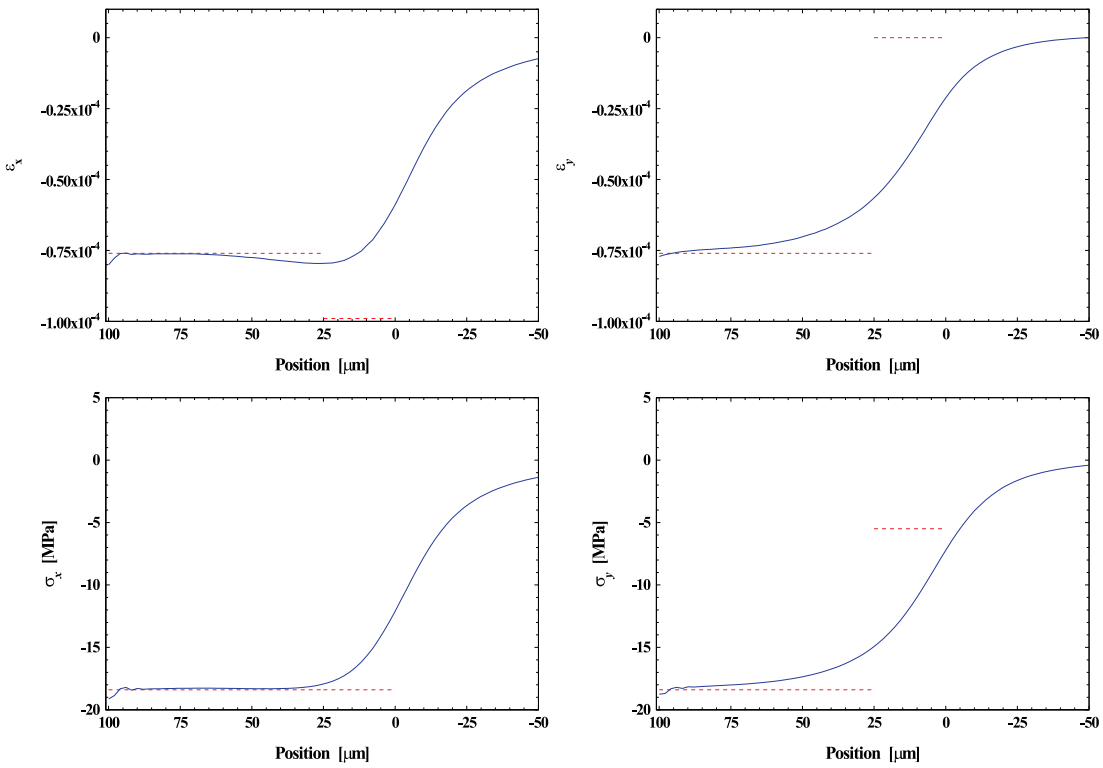


Figure 3.6: FEM calculation of stress and strain in a 1 μm thick silicon cantilever with a biaxially stressed 0.1 μm gold layer on top. The length and width are 100 μm and 50 μm. The plotted values are those found for the strain and the stress in the top of the silicon below the gold layer. The strain and the stress are plotted along the length axis with the clamp of the cantilever being at 0 μm and the apex of the cantilever at 100 μm. The analytical values are drawn with dotted lines with beam values (case C) for $x \geq w/2$ and with clamped values (case D) for $x < w/2$. The analytical formula is presented in equations 3.6-7 and 3.6-8 on page 30. The longitudinal(x) and transversal(y) FEM values are converging when moving away from the clamping. From 50 μm the difference between σ_x and σ_y is less than 5 % and the difference between ε_x and ε_y is less than 10 %.

μm. From 0 to -50 μm the strain and the stress in the support structure is shown.

It is clear from the graphs that the assumption of zero transversal strain at the clamp used in the analytical expressions does not hold. However, it is also found that for $x \gtrsim w$, the analytical beam model fits well to the FEM results, since the longitudinal and the transversal values are converging.

For both longitudinal strain and stress the FEM values are constant, and hence not affected by the clamping, for $x \gtrsim \frac{1}{2}w$. For the transversal strain and stress $x \gtrsim w$ before the effect of the clamping disappears.

Sader[65] has investigated the validity of the assumption of 'free' cantilever bending with an applied surface stress. The work focused on the effect of the clamping on deflection, slope and curvature of the cantilever, as this is of major interest when using optical readout, whereas in-plane deformation was not calculated. From the results it is also seen that the cantilever is affected near the clamping in an approximate range of $0 < x < w$ where for example the curvature in the free bending model is more than 20% off compared to a finite element model.

From the results of the FEM analysis it is concluded that for $x \gtrsim w$ the cantilever is, to a good approximation, behaving as a beam. So for $L \gg w$ the solution found in case C will be the best approximation to use when optimising for measuring surface stresses, as most of the cantilever will experience the beam boundary conditions. This will for example be the case for most cantilevers seen in the literature. For $L \lesssim w$ on the other hand, case D with the plate boundary conditions will be the appropriate model to use, though in order to get good quantitative results a FEM analysis is required.

The relative resistance changes - or sensitivities - for the four cases can be found by inserting ε_x and ε_y in equation 3.2-3. The results from this section are summarised in table 3.1.

Table 3.1: Results from case A-D. The relative resistance change is found from equation 3.2-3.

Case A	**Case C**
Apex force, beam	In-plane stress, beam
σ_x	σ_x
$\sigma_y = 0$	$\sigma_y = \sigma_x$
$\varepsilon_x = \frac{\sigma_x}{E}$	$\varepsilon_x = \frac{\sigma_x(1-\nu)}{E}$
$\varepsilon_y = \frac{-\nu\sigma_x}{E}$	$\varepsilon_y = \frac{\sigma_x(1-\nu)}{E}$
$\frac{\Delta R}{R} = \varepsilon_x[K_L(A-\nu B) + K_T(B-\nu A)]$	$\frac{\Delta R}{R} = \varepsilon_x[K_L + K_T]$
Case B	**Case D**
Apex force, plate	In-plane stress, plate
σ_x	σ_x
$\sigma_y = \nu\sigma_x$	$\sigma_y = \nu\sigma_x$
$\varepsilon_x = \frac{\sigma_x(1-\nu^2)}{E}$	$\varepsilon_x = \frac{\sigma_x(1-\nu^2)}{E}$
$\varepsilon_y = 0$	$\varepsilon_y = 0$
$\frac{\Delta R}{R} = \varepsilon_x[AK_L + BK_T]$	$\frac{\Delta R}{R} = \varepsilon_x[AK_L + BK_T]$

3.4 Minimum detectable signal

In order to estimate the performance of a sensor it is not enough to know the sensitivity of the sensor; the figure of merit is the signal to noise ratio. The minimum signal that can be measured when allowed for the noise and the sensitivity of the sensor, *i.e.* the resolution, will be presented in this section.

3.4.1 Readout principle

The resistance change of the piezoresistor is converted to a voltage change in a Wheatstone bridge configuration which is outlined in figure 3.7. The output

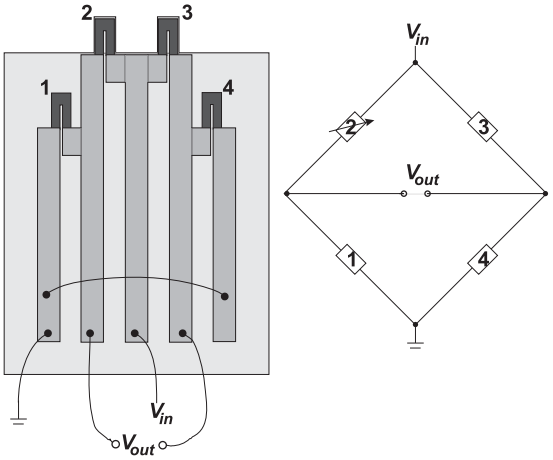


Figure 3.7: Basic design of the cantilever chip with four integrated piezoresistors placed in an on-chip Wheatstone bridge.

voltage from the Wheatstone bridge is

$$V_{out} = \frac{1}{4}\frac{\Delta R}{R}V_{in} \tag{3.4-1}$$

where V_{in} is the supply voltage. The chip has four on-chip piezoresistors two of which are placed on cantilevers. With this design one of the cantilevers is an 'active' cantilever reacting with the analyte in the sample, thus measuring the signal of interest, whereas the other cantilever is 'passive' and is filtering out the signals that are identical for both piezoresistors. These signals will for example include some mechanical noise and resistance changes caused by temperature drift. The effect of the on-chip Wheatstone bridge and the reference cantilever is investigated in detail in [23], where it is shown how this configuration reduces drift by two orders of magnitude compared to a sensor with no reference cantilever. The effect of this on-chip filtering has been illustrated by Christensen[66] and is shown in figure 3.8. The figure shows the output signal from the Wheatstone

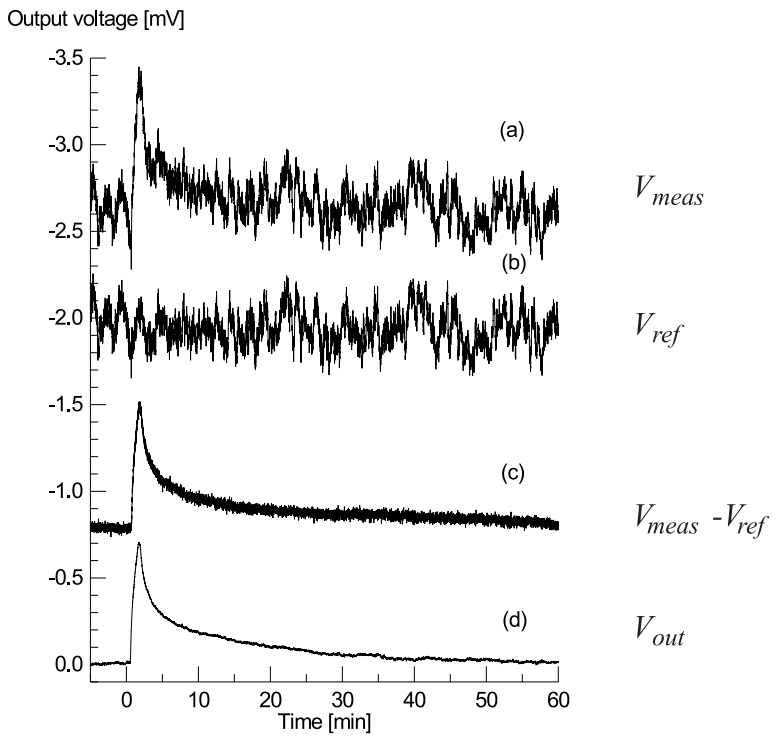


Figure 3.8: Measurement of the absorption and the desorption of methanol in a polymer layer on the measurement cantilever[66]. Curve (a) shows the voltage signal from the measurement cantilever and curve (b) shows the signal from the reference cantilever. Curve (c) shows the result of subtracting the two signals off-chip, while curve (d) shows the on-chip signal from the Wheatstone bridge.

bridge and the separate signals from the measurement cantilever and the reference cantilever. It is clearly illustrated how the reference cantilever is filtering the common mode noise for the two cantilevers and thereby reducing the noise on the measurement signal.

3.4.2 Resolution

The sensitivity when measuring an apex force can be represented by $\frac{\Delta R}{R} z^{-1}$ and the sensitivity when measuring a surface stress can equivalently be represented by $\frac{\Delta R}{R} \sigma_s^{-1}$. They are measures of the relative resistance change per unit bending z or per unit surface stress σ_s, respectively. In order to find the minimum detectable bending or surface stress, it is assumed that the minimum detectable output voltage equals the voltage signal caused by noise $V_{out\ min} = V_{noise}$. Then from equation 3.4-1 the minimum detectable bending z_{min} and surface stress $\sigma_{s\ min}$

are

$$z_{min} = \frac{V_{noise}}{\frac{1}{4}(\frac{\Delta R}{R}z^{-1})V_{in}} \quad (3.4\text{-}2)$$

$$\sigma_{s\ min} = \frac{V_{noise}}{\frac{1}{4}(\frac{\Delta R}{R}\sigma_s^{-1})V_{in}} \quad (3.4\text{-}3)$$

These are measures of the resolution of the sensor with respect to bending and surface stress. The nature of the two different scenarios will be expressed through the dependence of $\frac{\Delta R}{R}$ on the strain and will be investigated in sections 3.5 and 3.6.1.

3.4.3 Noise sources

As for noise sources, only inherent noise in the sensor device is considered. These noise sources include thermal mechanical noise and the two electrical noise sources, Johnson noise and 1/f noise.

Johnson noise

Johnson noise is caused by thermal fluctuations of the charge carriers. The Johnson voltage noise of a resistor with resistance R is given by

$$V_J = \sqrt{4k_BTR\Delta f} \quad (3.4\text{-}4)$$

where Δf is the measured bandwidth, k_B is Boltzman's constant, and T is the absolute temperature.

1/f noise

1/f noise is electrical noise that falls off at high frequencies. Hooge *et al.*[67] has described a model in which the spectral noise density S is inversely proportional to the number of carriers N in the resistor

$$S_{1/f} = \frac{\alpha V_s^2}{fN} \quad (3.4\text{-}5)$$

where V_s is the applied voltage, α is a material parameter, and f is the frequency.

Harley *et al.*[15] has used this model on cantilevers with silicon piezoresistors and confirmed the dependence on the number of charge carriers. The material parameter α is very dependent on annealing, and for single crystalline silicon the value will maybe be as low as $10^{-6} - 10^{-5}$[68, 25]. In the work presented later in this thesis, α values for polysilicon between $9 \cdot 10^{-4}$ and $8 \cdot 10^{-2}$ depending on annealing have been found.

The 1/f voltage noise $V_{1/f}$ in the frequency range f_{min} to f_{max} is found from equation 3.4-5

$$V_{1/f} = \sqrt{\frac{\alpha V_s^2}{N} \ln\left(\frac{f_{max}}{f_{min}}\right)} \tag{3.4-6}$$

Thermal vibrational noise

The thermal vibrational noise that is picked up in a piezoresistive AFM cantilever is described by Hansen *et al.*[69] in detail. The deflection noise z_v for the first vibrational mode of the cantilever is approximately[69, 70]

$$z_v \approx \sqrt{\frac{k_B T}{k}} \tag{3.4-7}$$

To find the relevance of this noise when piezoresistive readout is used to measure surface stress, this approximative value for the deflection noise is converted to a surface stress noise σ_{sv} as

$$\sigma_{sv} = k_{\sigma_s} z_v = \frac{2EI}{wdL^2} z_v \tag{3.4-8}$$

where $H/2$ from equation 3.1-20 is replaced by d, which is the distance from the piezoresistor to the neutral plane of the cantilever. If a white noise distribution is assumed, the noise picked up in the frequency interval Δf is scaled as

$$\sigma_{sv_{\Delta f}} = k_{\sigma_s} \sqrt{\frac{k_B T \Delta f}{k f_{\text{res}}}} \tag{3.4-9}$$

This is a worst case value, since the vibration energy will be concentrated around the resonant frequency. If the frequency distribution of the vibrations is considered, the off-resonance deflection noise is approximated by[71, 72]

$$z_v \approx \sqrt{\frac{2k_B T \Delta\omega}{\pi k Q \omega_{res}}} \tag{3.4-10}$$

or a factor $(\frac{1}{2}\pi Q)^{-\frac{1}{2}}$ lower than the white noise approximation, and it is obvious that cantilevers with high Q factors will have a low off-resonance vibration noise.

This thermal noise contribution is dependent on both the geometry and the measured bandwidth. For the sensors developed in this project, the thermal surface stress noise is assumed to have no influence. Even for the SOI sensor presented in chapter 6, the minimum detectable surface stress is an order of magnitude higher than the white surface stress noise from equation 3.4-9.

Total noise

The total noise is averaged as

$$V_{noise} = \sqrt{V_J^2 + V_{1/f}^2 + V_v^2} \tag{3.4-11}$$

where the last term for the thermal vibrational noise can be omitted for most situations.

For optical readout the only of the above mentioned noise sources that concerns the cantilever design is the thermal mechanical noise. In this case a long soft cantilever gives the highest sensitivity, and the spring constant should be kept high enough to keep the thermal vibrations under a desired application specific minimum. For piezoresistive readout the picture is not as simple, as the electrical as well as the mechanical properties of the piezoresistor and cantilever influence the design and the optimal resolution.

To do an optimisation of the performance of the piezoresistive sensor, the strain in the piezoresistor has to be found, and this will be dealt with in the following sections.

3.5 Apex force

In calculating the strain of a piezoresistor in a cantilever with an apex force applied, it is assumed that we obtain pure bending of the cantilever, thus neglecting axial elongation. This is the kind of strain an AFM cantilever experiences when pressed against a surface during scanning. For a beam such as case A in section 3.3, the radius of curvature ρ_x is given by [62]

$$\frac{1}{\rho_x} = \frac{F(L-x)}{EI} \tag{3.5-1}$$

where F is a force acting on the apex of a cantilever of length L as shown in figure 3.9. With the z axis in the same direction as F, the strain is

$$\varepsilon_x = -z/\rho_x \tag{3.5-2}$$

With the origin of the z axis being the neutral plane and d being the distance from the neutral plane to the resistor, the strain in the resistor is

$$\varepsilon_{x\ res} = \frac{F(L-x)}{EI} d \tag{3.5-3}$$

which averaged over the resistor of length λ sketched in figure 3.9 gives

$$\bar{\varepsilon}_{x\ res} = \frac{1}{\lambda} \int_0^{\lambda} \frac{F(L-x)d}{EI} dx = \frac{F(L-\frac{\lambda}{2})}{EI} d \tag{3.5-4}$$

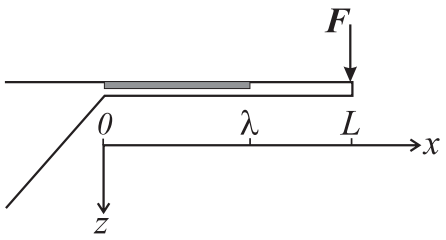


Figure 3.9: Force acting on the apex of a cantilever. λ represents the length of an integrated piezoresistor.

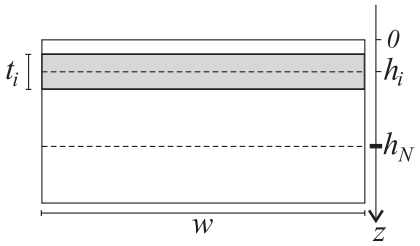


Figure 3.10: Cross section of cantilever with the i'th layer shaded. h_N and h_i are the positions of the neutral plane and the i'th layer, respectively. w is the width of the cantilever and t_i is the thickness of the i'th layer.

For a multilayered cantilever, which almost inevitably will be the case with piezoresistive readout, the neutral plane h_N is found as

$$h_N = \frac{\sum_i E_i h_i t_i}{\sum_i E_i t_i} \tag{3.5-5}$$

where h_i is the position, t_i is the thickness, and E_i is the Young's modulus of the i'th layer, see figure 3.10. EI for the multilayered cantilever is found from $\Sigma_i E_i I_i$, where I_i is the area moment of inertia for the i'th layer, as described by

$$\begin{aligned} I_i &= \int_A z^2 dA \\ &= \int_{h_i - h_N - t_i/2}^{h_i - h_N + t_i/2} z^2 w dy \\ &= \frac{w t_i^3}{12} + w t_i (h_i - h_N)^2 \end{aligned} \tag{3.5-6}$$

where A is the area of the cross section, w is the width of the beam and $h_i - h_N$ is the distance between the i'th layer and the neutral plane of the beam.

Now, substituting F by kz in equation 3.5-4 and using table 3.1, it will follow

that the bending sensitivity is

$$\frac{\Delta R}{R} z^{-1} = \frac{k(L - \frac{\lambda}{2})d}{EI}[K_L(A - \nu B) + K_T(B - \nu A)] \tag{3.5-7}$$

If the resistance parallel to the length axis of the cantilever dominates so $A \gg B$ and Poisson contraction is ignored, then the often used description[15, 18, 73]

$$\frac{\Delta R}{R} z^{-1} = \frac{k(L - \frac{\lambda}{2})d}{EI} K_L \tag{3.5-8}$$

of the sensitivity is obtained.

3.6 In-plane stress

The objective in this section is to find the strain $\varepsilon_{x\ res}$ in the piezoresistor which can then be inserted in equations 3.2-3 and 3.4-3 to obtain the minimum detectable surface stress. The model is developed by O. Hansen[74] and describes a multilayered cantilever with built-in stress.

The strain in the cantilever is considered to consist of an axial term ε_0 giving elongation/contraction and a term giving the strain when the cantilever bends βz (equivalent to equation 3.5-2) so

$$\varepsilon = \varepsilon_0 + \beta z \tag{3.6-1}$$

where z is the distance to the neutral axis of the cantilever. The strain ε equal to ε_x used in the previous sections, but since the strain is isotropic in the xy-plane the subscript is omitted. The stress is then

$$\sigma = \sigma_i + \varepsilon Y_i \tag{3.6-2}$$

where σ_i is the built-in stress the i'th layer. Y_i is the biaxial modulus $E_i/(1 - \nu_i)$ for a beam and Y_i is the plate modulus $E_i/(1 - \nu_i^2)$ for a plate following the discussion in section 3.3. To solve for ε_0 and β the following equilibrium conditions are used

$$F = \int \sigma dz = 0 \text{ and } M = \int z\sigma\, dz = 0 \tag{3.6-3}$$

where F and M are the total force and bending moment per unit width, respectively. The origin of the z-axis is the neutral plane of the cantilever. The position of the top z_T of the cantilever is found from

$$z_T = \frac{\sum_{i=0}^{n} E_i t_i h_i}{\sum_i E_i t_i}, \tag{3.6-4}$$

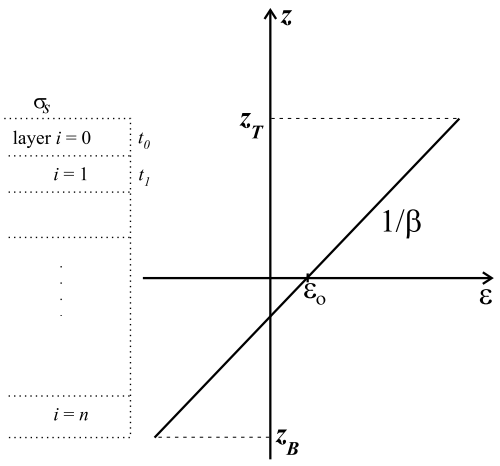


Figure 3.11: Strain distribution through the cantilever.

where t_i is the thickness of the i'th layer and $h_i = \sum_{j=0}^{i} t_j - \frac{t_i}{2}$ is the distance from the top of the cantilever to the middle of the i'th layer, see figure 3.11. Equation 3.6-3 can now be written as the sum of the integration over each layer

$$F = \sum_{i=0}^{n} \sigma_i t_i + \varepsilon_0 \sum_{i=0}^{n} Y_i t_i + \beta \sum_{i=0}^{n} Y_i \frac{z_{iT}^2 - z_{iB}^2}{2} = 0 \tag{3.6-5}$$

$$M = \sum_{i=0}^{n} \sigma_i \frac{z_{iT}^2 - z_{iB}^2}{2} + \varepsilon_0 \sum_{i=0}^{n} Y_i \frac{z_{iT}^2 - z_{iB}^2}{2} + \beta \sum_{i=0}^{n} Y_i \frac{z_{iT}^3 - z_{iB}^3}{3} = 0 \tag{3.6-6}$$

where z_{iT} and z_{iB} denotes the top and the bottom of the i'th layer, respectively. The strain as function of the built-in stress is then

$$\varepsilon_o = -\frac{\Sigma_i \sigma_i t_i}{\sum_i Y_i t_i} \tag{3.6-7}$$

$$\beta = -\frac{\Sigma_i \sigma_i t_i \left(z_T - \sum_{j=0}^{i} t_j + \frac{t_i}{2} \right)}{\sum_i Y_i t_i \left((z_T - \sum_{j=0}^{i} t_j + \frac{t_i}{2})^2 + \frac{1}{3}(\frac{t_i}{2})^2 \right)} \tag{3.6-8}$$

It is evident that the strain is only a function of the materials through Y and of the thicknesses of the layers, whereas the width and length of the cantilever do not have an influence on the strain.

3.6.1 Surface stress

The applied in-plane stress considered here will be that caused by a uniform surface stress on the cantilever. Stresses in all layers except in the top layer will be discarded, since we are interested in the strain change caused by a surface

stress and not the 'off-set' strain caused by the stress in the cantilever. The surface stress σ_s (with the units of N/m) is introduced as $\sigma_s = \sigma_{top} t_{top} \neq 0$ as $t_{top} \rightarrow 0$. With this the expressions for the strain reduces to

$$\varepsilon_o = -\frac{\sigma_s}{\sum_i Y_i t_i} \tag{3.6-9}$$

$$\beta = -\frac{\sigma_s z_T}{\sum_i Y_i t_i \left((z_T - \sum_{j=0}^{i} t_j + \frac{t_i}{2})^2 + \frac{1}{3}(\frac{t_i}{2})^2 \right)} \tag{3.6-10}$$

It can be seen from the strain distribution through the cantilever (figure 3.11 and the above expression for ε) that the neutral plane in $z = 0$ defined through equation 3.6-4 is not strain free when there is a built-in stress (here surface stress) in the cantilever. Rather, the effective neutral plane shifts away from the surface with the surface stress.

What this means when designing a cantilever sensitive to measuring surface stress will be shown next for a case with a simple cantilever geometry.

Surface stress in simple cantilever

The strain in a cantilever consisting of a single layer and with a surface stress on the top surface is

$$\varepsilon = -\frac{\sigma_s}{Yt} - \frac{6\sigma_s}{Yt^2} z \tag{3.6-11}$$

The strain at the top surface ε_T and the strain at the bottom surface ε_B are then

$$z = t/2: \quad \varepsilon_T = -\frac{4\sigma_s}{Yt} \tag{3.6-12}$$

$$z = -t/2: \ \varepsilon_B = \frac{2\sigma_s}{Yt} \tag{3.6-13}$$

This is illustrated in figure 3.12. In the figure it is also shown how the effective neutral axis is situated 2/3 of the thickness away from the surface instead of 1/2 of the thickness as for the stress free cantilever. The importance of including the elongation/contraction term ε_0 in the expression for the strain is illustrated by the fact that it constitutes 25 % of the strain at the top surface. In addition, if this contribution was omitted in a pure bending approximation, the model would have shown that the strain is symmetric in the cantilever.

For the simple structure the strain at the top surface is twice as high as the strain at the bottom surface. The general conclusion for any cantilever is that in order to obtain a large resistance change and thus a high sensitivity, the piezoresistor should be placed as close to the surface with the applied surface stress as possible.

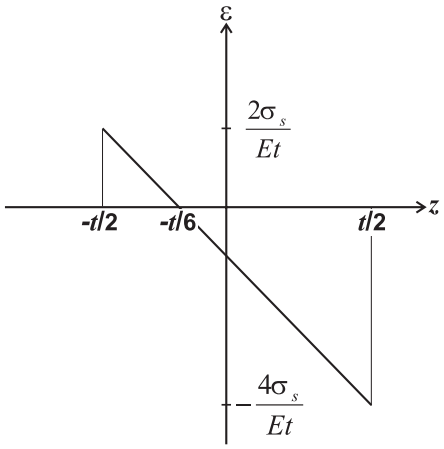


Figure 3.12: Strain as a function of position inside simple cantilever with a surface stress. The surface stress is on the top surface at $z = t/2$. The effective neutral axis where $\varepsilon = 0$ is at $z = -t/6$.

With a surface stress of equal magnitude on both the top and the bottom surface of the cantilever, the strain in the simple cantilever is

$$\varepsilon = \varepsilon_0 = -\frac{2\sigma_s}{Yt} \tag{3.6-14}$$

or half the strain at the top surface with only surface stress on one side. In this symmetric case the cantilever is only stretched or contracted, but in general the cantilever will bend.

For the general case, the most sensitive sensor is obtained if measuring differential stress between the two sides of the cantilever, *i.e.* in praxis the task will be to make the molecules of interest bind to one surface, whereas the other surface in the ideal case should be inert to any binding.

3.7 Summary

In this chapter the design of the silicon piezoresistors used in the Bioprobe project was presented followed by a description of the readout principle.

Following from this, the different strains encountered for cantilever beams and plates were described, and analytical expressions for the influence on the sensitivity was calculated. It was justified with a FEM analysis that the beam approximation will hold for most cases, but that it is a function of the geometry through the clamping of the cantilever since for example the strain of a short piezoresistor placed close to the support is strongly influenced by the clamp.

The noise sources influencing the readout signal were introduced. Together with the presented derivations of the strain in the piezoresistor as a function of either a apex force or a surface stress, a description of the minimum detectable signal from the piezoresistive sensor was found, and this measure of the resolution will be the basis for optimising the design of the cantilever sensors presented in this thesis.

To optimise the sensitivity in general, the binding of molecules, and hence the build-up of a surface stress, should preferably be limited to one surface of the cantilever, and the piezoresistor should be placed as close to the position of the surface stress as possible.

Chapter 4

Process optimisation

This chapter will describe the preliminary tests that were made before a complete process sequence for the sensor could be suggested. The chapter will mainly deal with the process of making the titanium silicide wiring and the coating hereof, but it will also contain tests with highly doped silicon wiring.

The test of the quality of the coating on the wires will be that they can stand 20 min in 80°C KOH. The chips will all go through an etching step in KOH, as the cantilevers are release-etched in KOH from the back of the wafer. It is estimated that even with a holder that protects the front of the wafer, the front will be exposed to the KOH for about 20 min since the etch is not totally uniform over the wafer. At the same time as being process relevant, the test is also a very tough test that only allows coatings with good step coverage, good adhesion, and high chemical durability, such as LPCVD silicon nitride, to pass. After passing this liquid protection test, the next criterion is that the on-chip electrical circuit, *i.e.* the wiring and the resistors, survive the coating process, and can be accessed by etching contact holes in the coating.

4.1 Titanium silicide

Titanium silicide has been used in the semiconductor industry for making ohmic contacts and as gates and interconnections[75]. Titanium silicide belongs to a group of silicides called intermetallic silicides as they have metallic properties. Among the intermetallic silicides titanium silicide and cobalt silicide have the lowest resistivities. As titanium moreover is readily available in MIC's clean-room, titanium silicide was the first choice for making silicide wiring on the chips. As mentioned in the previous chapter the titanium silicide is stable at high temperatures and can be coated in an LPCVD process, but this prerequisite is met by many, if not most, of the intermetallic silicides[75].

4.1.1 Processing of titanium silicide

The titanium silicide is formed by evaporating a titanium layer on top of a silicon layer and then heat it by rapid thermal annealing (RTA) in an argon atmosphere. For the purpose here all silicides were formed on amorphous silicon or polysilicon on top of either silicon oxide or silicon nitride layers that acts as insulation to the silicon substrate.

The process sequence is illustrated in figure 4.1. First a silicon nitride and then an amorphous silicon is deposited. The silicon is patterned with reactive ion etching (RIE) and after a short dip in buffered hydrofluoric acid (BHF) to remove the native oxide, the titanium layer is deposited. The wafer is put in an RTA oven

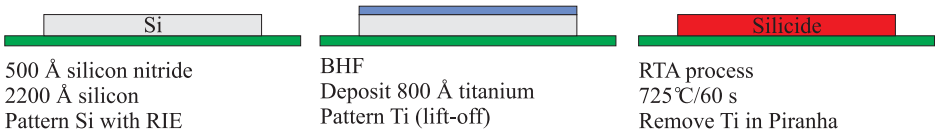


Figure 4.1: Process sequence for titanium silicide.

and purged with argon for 10 min before the anneal. If this purging is omitted a milk-white silicide of poor quality is obtained because of oxidation during the anneal. In literature the reported anneal temperatures are about 800°C, but it was seen from the experiments that much lower nominal temperatures in the RTA oven were sufficient to achieve resistivities at about 20 μΩ·cm. This was attributed to the fact that the optical pyrometer temperature measurement of the RTA oven is a 'bulk' measurement giving the temperature of the wafer, and the silicon/titanium stack is deposited on a thermally insulating layer so the top thin film is warmer than the average temperature of the wafer. As an example the low resistivity phase was reached at nominally 625°C, when the silicide was made on a 4300 Å silicon oxide layer.

In the first tests with the titanium silicide, the polysilicon was structured on top of a silicon oxide layer and titanium was then deposited on the wafer. The titanium then covered the whole wafer during the RTA process. The titanium on top of silicon will then form titanium silicide and the rest of the titanium will afterwards be etched away in Piranha[1] which does not attack the titanium silicide. Simple as it is this so called self-aligned process, it was found to have some drawbacks. In the first tests with silicon oxide as the insulator, a line width degradation of a few μm was observed as shown in figure 4.2. Silicon is the interdiffusing species when making titanium silicide and silicon diffusion was suspected to cause this effect. No action was taken at this point, because as long

[1] H_2SO_4 and H_2O_2

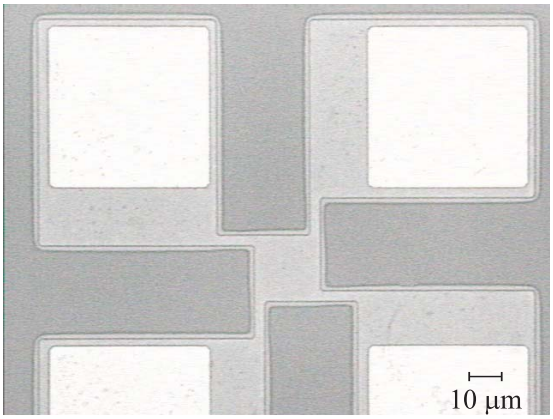


Figure 4.2: SEM picture showing a titanium silicide Van der Pauw test structure. The light grey structure is the titanium silicide and the innermost line shows the original silicon structure. The white squares are metal contact pads.

as the effect is known it can be accounted for when making the mask lay-out. When silicon nitride later was used as the insulating layer, because the cantilever sensor is made of silicon nitride as depicted in figure 2.1, it was found that the titanium silicide wires were short circuited. This is probably due to formation of titanium nitride on the silicon nitride surface. A lift-off process of the titanium was introduced to replace the self-aligned process to prevent any reaction between the titanium and the silicon nitride.

Haken *et al.*[76] report that annealing in nitrogen will reduce silicon diffusion because nitrogen will diffuse into the titanium silicide and form titanium nitride at the grain boundaries, which reduces the diffusion of the silicon. Since the titanium silicide is to be formed on silicon nitride, and the lift-off process therefore is necessary, no change in ambient gas in the RTA oven was made since the lift-off process also prevents the loss of line width through silicon diffusion.

Process limitations

The thickness of the titanium silicide is a limiting factor in the sense that it is not possible to make arbitrary thick layers. This is due to the large stresses obtained in titanium silicide, that will make thick layers peal off. Therefore the thickness of the silicide is an important parameter to control. And in order to calculate the resistivity of the titanium silicide, the thickness is also a needed parameter. The thickness and the stress of the titanium silicide was thus investigated.

The volume fraction between titanium silicide and titanium vol_{TiSi_2}/vol_{Ti} is 2.44 (see table 4.1). Secondary ion mass spectroscopy (SIMS) was used for measuring the actual obtained thickness of the titanium silicide. A test wafer was prepared

	ρ [g/cm^3]	M [g/mol]
Ti	4.54	48.12
Si	2.33	28.19

and with $\rho_{TiSi_2} = 4.04$ g/cm^3:

Molar volumes [cm^3/mol]

Ti	Si	$TiSi_2$
10.60	12.10	25.87

1 Å Ti + 2.28 Å Si → 2.44 Å $TiSi_2$

Table 4.1: Volume ratios between silicon, titanium and titanium silicide.

with titanium silicide formed directly from the bulk silicon, as an insulating layer under the silicide could upset the measurement due to charging of the sample. This also means that the deposited 1000 Å thick titanium layer was the limiting parameter and that a silicide thickness of 2400 Å was obtainable in principle. The thickness of the titanium silicide layer was measured at 1500 Å - see figure 4.3 - *i.e.* much less than the 2400 Å. It is assumed that all the titanium silicide wiring made in this project has this thickness. The resistivities calculated with this thickness are around 20 μΩ·cm in accordance with the value found in the literature, it would therefore appear that the assumption is sound.

Wafer curvature measurements were made to calculate the stress in the titanium silicide using Stoney's equation[77]

$$\sigma = \frac{EH^2}{(1-\nu)6Rh} \tag{4.1-1}$$

where H is the wafer thickness, h is the titanium silicide thickness, and R is the radius of curvature of the wafer. A tensile stress of 1.5 GPa was found. With the purpose of making cantilevers in mind, the titanium silicide should not be used on free hanging structures, since the large stress could make them bend, rather it should be confined to the substrate.

4.1.2 Interfacing titanium silicide and silicon

The design idea is to use the titanium silicide wiring as interconnects for the silicon piezoresistors on the chip. The piezoresistors are doped with ion implantation and for this reason the effect of implantation on the titanium silicide has been tested.

Basically two schemes were tested and their process sequences are shown in figure 4.4. In (A) the implantation with boron is made after the formation of the

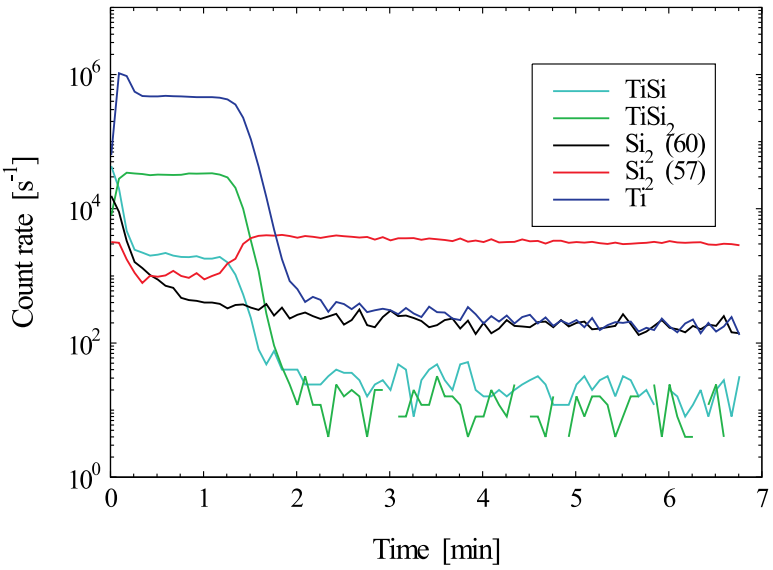


Figure 4.3: SIMS on titanium silicide made from 1000 Å of titanium on a silicon wafer. Calibrations show that 1.5 min corresponds to 1550 Å. From 1 min to 1.5 min the count rate for titanium falls almost an order of magnitude, indicating a thickness of about 1500 Å for the titanium silicide layer.

titanium silicide. In (B) the titanium is patterned and works as an implantation mask, and the titanium silicide is formed after the implantation. Both processes produced titanium silicide with a low resistivity at around 20 μΩ·cm. In process (A) the resistivity of the titanium silicide increased to 70 μΩ·cm but a second anneal step could restore the resistivity to the pre-anneal value.

The measurement on the test structure revealed that the resistance between the silicon and the titanium silicide was very high - in the 10-100's of kΩ range. A first guess was that the silicon near the silicon/silicide interface simply diffused into the silicide making a void at the interface. In a test with thinner titanium silicide made of 400 Å titanium on 2200 Å silicon, where the titanium silicide as a upper limit should have a thickness of less than 1000 Å, the resistance was still high. This indicates that the problem more likely is linked to diffusion of the boron.

In the literature the diffusion of boron to the silicon/titanium silicide interface is studied in detail. Kalnitsky *et al.*[78] report that boron diffuses to the silicon/silicide interface where titanium boride is formed. The titanium boride layer and the depletion of the silicon near the interface then account for the high resistance. Choi *et al.*[79] and Maex[80] report on the same, and Maex shows how the formation of TiB_2 from boron doped silicon and $TiSi_2$ is energetically favorable. In these articles it is stated that the boron is almost immobile in the silicide.

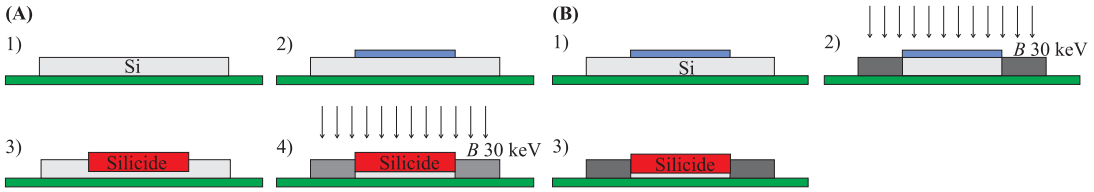


Figure 4.4: Implantation tests with titanium silicide.
In (A) a titanium layer is formed so that it partly covers a silicon wire(2). Titanium silicide is made with an RTA process(3), and implantation with boron is made(4). In order to restore the low resistivity of the titanium silicide a second RTA is necessary. In (B) a titanium layer again partly covers a silicon wire(1), and then the implantation is made(2). The titanium silicide is formed with an RTA process(3).
Both processes give a low resistivity of the titanium silicide of 20 $\mu\Omega$·cm.

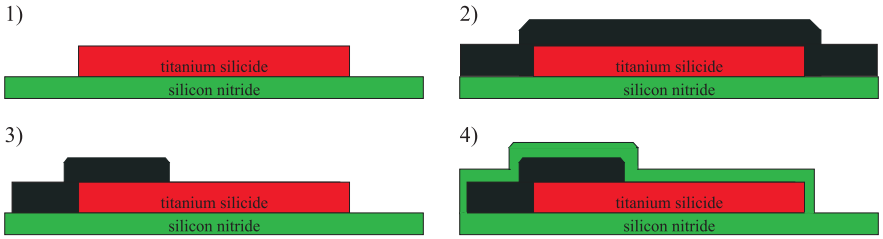


Figure 4.5: Process sequence for testing titanium silicide wiring and silicon resistors made in separate silicon layers.
(1) The titanium silicide wiring is patterned and formed.
(2) LPCVD poly silicon is deposited and implanted with boron.
(3) The silicon resistor is formed with an RIE process.
(4) LPCVD silicon nitride is deposited and an RTA at 900°C for 60 s is performed to activate the dopant.
As a last step the top silicon nitride is stripped away in an RIE process with N_2 and CHF_3.

Twiford *et al.*[81] on the other hand claim that the diffusion of boron through titanium silicide is very fast but if a controlled pile-up of dopant near the interface can be made, the interface contact resistance can be minimised.

Whether it is caused by the formation of titanium boride at the interface or a fast diffusion through the titanium silicide, it seems reasonable that the high contact resistance is caused by the depletion of dopant near the interface. With a high contact resistance between the silicon and the titanium silicide, a solution could be to make a large interface area. This was tried by making the silicon resistors and the titanium silicide in two silicon layers as sketched in figure 4.5. The titanium silicide layer is processed first in order to minimise the thermal budget for the dopant in the silicon. In order to further reduce the thermal budget the dopant is activated by an RTA process in stead of a conventional furnace

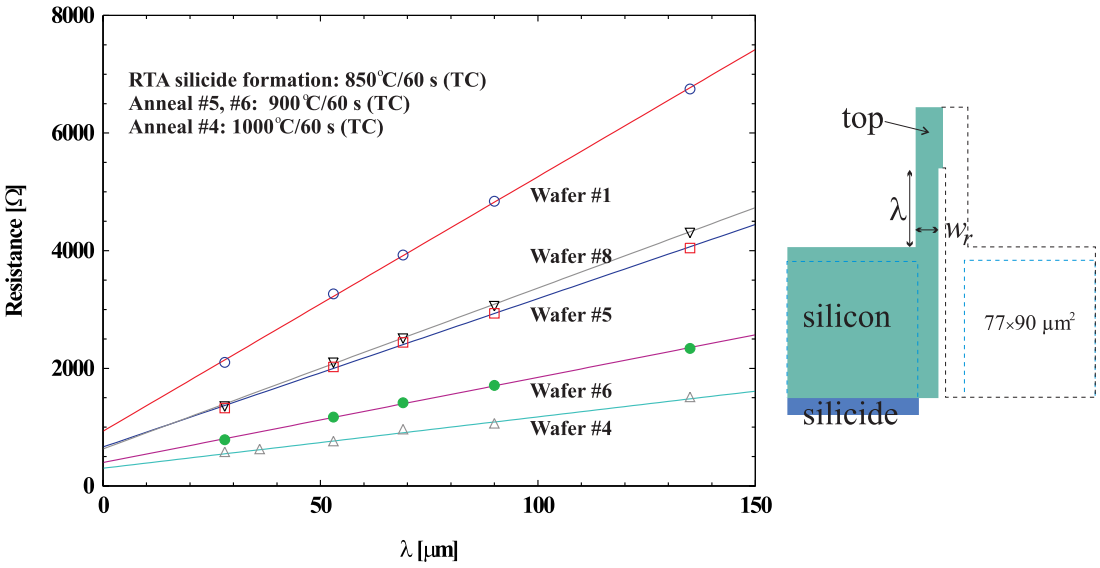


Figure 4.6: Left: Resistance as a function of resistor length λ. Right: Geometry of resistor.
'No anneal' means that the only annealing is the deposition of silicon nitride (835°C for 40 min).

annealing. The wiring and resistor are coated with an LPCVD silicon nitride before the RTA and therefore this furnace process is a default annealing for the dopant activation. The test mask contained resistors of different lengths and the resistance as a function of the resistor length λ is shown in figure 4.6. The RTA temperature at 900°C is the nominal temperature, the real temperature of the thin films is higher. The intersection at $\lambda = 0$, R_{int}, represents the spreading

Wafer	Dose [cm^{-2}]	RTA	R_{int} [Ω]	$R_\square$ [Ω]	ϱ [Ω·cm]	R_c [Ω]	ϱ_c [Ω·cm^2]
#1	$5 \cdot 10^{15}$	-	932	521	$1.3 \cdot 10^{-2}$	260	$1 \cdot 10^{-4}$
#5	$5 \cdot 10^{15}$	900°C/60 s	663	312	$7.6 \cdot 10^{-3}$	254	$5 \cdot 10^{-5}$
#8	10^{16}	-	630	340	$8.2 \cdot 10^{-3}$	191	$9 \cdot 10^{-5}$
#6	10^{16}	900°C/60 s	398	181	$4.3 \cdot 10^{-3}$	165	$3 \cdot 10^{-5}$
#4	10^{16}	1000°C/60 s	302	108	$2.6 \cdot 10^{-3}$	163	-

Table 4.2: Sheet resistances $R_\square$ are measured on Van der Pauw structures. The resistivity ϱ is found from $\varrho = R_\square t$, with t=240 nm being the thickness of the silicon. The contact resistance is found from equation 4.1-2 as $R_c = R_{int} - 1.29R_\square$. The specific contact resistance ϱ_c is found from $\varrho_c = R_K A$, with the resistance R_K measured on Kelvin structures with contact area A.

resistance and the contact resistance at the silicon/wiring interface and the resistance of the top half of the resistor, see figure 4.6. By finite element calculations the spreading resistance from the resistor to the wiring and the resistance of the

top half of the resistor is found at 0.69 and 0.60, respectively:

$$R = R_{\square}(\frac{\lambda}{w} + 1.29) + R_c \tag{4.1-2}$$

where $R_{\square}$ is the sheet resistance and R_c is the contact resistance. It can be seen from table 4.1.2 how both resistivity and contact resistance goes down with increasing doping dose and annealing. From the specific contact resistance, ϱ_c, it can be seen that the effective contact area is something like

$$\frac{\varrho_c}{R_c} \approx \frac{5 \cdot 10^{-5}\ \Omega \cdot \mathrm{cm}^2}{200\ \Omega} = 25\ \mu\mathrm{m}^2. \tag{4.1-3}$$

A way to increase this effective area is to increase the width, w_r, of the resistor leg. At the same time this will probably lower the spreading resistance at the contact area.

LPCVD silicon nitride coating

In the above test for contact resistance the wires and resistors were coated with an LPCVD silicon nitride coating. The silicon nitride is stripped off in an RIE process with N_2 and CHF_3 before measuring the resistances. An increase of the titanium silicide wiring resistance after the nitride strip of 50 to 100 % was found to be acceptable since the RIE attacked all of the wire. In a process sequence with custom made masks, the only titanium silicide that is etched by the RIE is that at the contact holes.

Other wafers with titanium silicide wiring were coated with LPCVD nitride and tested with success in 80°C KOH for 30 min.

4.2 Silicon wiring

Tests with silicon wiring were made along with the tests with the titanium silicide wiring. Three different techniques for making high doped silicon wires were tested:

- Implantation with an ion-implanter.
- In situ doping in an LPCVD furnace.
- Deposition of a highly doped boron-glass layer

The ion implantation technique has a very well controlled implantation dose. The drawback is that it is a serial time consuming technique. The in situ doping is faster as the dopant is incorporated in the silicon during deposition. The

Wiring	Anneal	ϱ_{wiring}	$\varrho_{\text{resistor}}$
in situ	1000 °C/20 min	$8.1 \cdot 10^{-3}$	$7.3 \cdot 10^{-3}$
in situ	950 °C/1 min	$9.5 \cdot 10^{-3}$	$7.4 \cdot 10^{-3}$
implant	835 °C/12 min	$6.0 \cdot 10^{-3}$	$16.7 \cdot 10^{-3}$
implant	1000 °C/20 min	$7.1 \cdot 10^{-3}$	$7.9 \cdot 10^{-3}$
boron-glass	835 °C/12 min	$6.8 \cdot 10^{-4}$	-
boron-glass	1000 °C/20 min	$6.4 \cdot 10^{-4}$	-
boron-glass	1000 °C/1 min	$6.7 \cdot 10^{-4}$	-
titanium silicide	950 °C/1 min	$20 \cdot 10^{-6}$	

Table 4.3: Tests with silicon wiring. For the in situ wiring 1.1 µm of silicon were deposited. The implanted wires are implanted with 10^{21} cm^{-3}. The resistors are in all cases poly silicon with a dopant concentration of $2 \cdot 10^{20}$ cm^{-3}. For the boron-glass process the resistors were shortcircuited by the wiring. The titanium silicide is shown as a comparison.

boron-glass technique can make much thicker implanted layers than the other two techniques as it drives the dopant in to the silicon while continuously supplying new dopant from the glass at the surface of the silicon. The process used here produced wires with a thickness of 5-7 µm.

The process sequences for the tests are in appendix F. The results are summed in table 4.3. With the test masks the boron-glass processed wires shortcircuited the resistor because of boron diffusion. Nevertheless, this technique can produce wiring with a resistance comparable to that of titanium silicide since it has a resistivity that is about a factor of 30 higher than titanium silicide and at the same time has a thickness that is 30 times bigger. The wires, however, are made directly in the bulk single crystalline silicon, and this accounts for the very low resistivity compared to the other silicon wiring techniques. Wiring made in the bulk silicon is also only isolated with a pn-junction that allows small leak currents to run.

All the above silicon wires were coated with 500 Å silicon nitride before annealing and subsequently tested in 80°C KOH for 30 min with no problems.

4.3 Summary

The processing of the titanium silicide wiring was optimised. Silicon diffusion causing line width degradation and titanium nitride formation was prevented by introducing a lift-off process for the titanium.

A high contact resistance between the silicon resistor and the titanium silicide was found. This is probably caused by the diffusion of boron to the interface where it forms titanium boride and thereby creates a depletion of the contact region below the interface. In order to reduce the contact resistance to an ac-

ceptable level, the silicide and the resistors need to be made of separate silicon layers, making it possible to make a large interface area.

It was decided that in order to minimise diffusion of boron, the silicide wiring should be made before the silicon resistors. In another attempt to minimise the thermal budget RTA was investigated for the activation of the dopant, and it was found to effectively activate the boron.

The titanium silicide was coated with LPCVD silicon nitride. The silicon nitride can be removed with an RIE process selectively to the silicide so that contact holes can be opened in the silicon nitride.

Different silicon wire schemes were tested, but only wiring made in the bulk single crystalline silicon could match the silicide with respect to a low series resistance, and it lacks the efficient insulation of the silicide encapsulated in silicon nitride.

Chapter 5

Surface stress sensor

This chapter will describe the design, realisation and testing of the cantilever sensor optimised for use in wet biochemical measurements. This has been an iterative process with process changes between the different batches.

5.1 The 1st generation

The general design is as described in chapter 2 combined with the titanium silicide wiring, see figure 5.1. Both titanium silicide wiring and the silicon piezoresistors

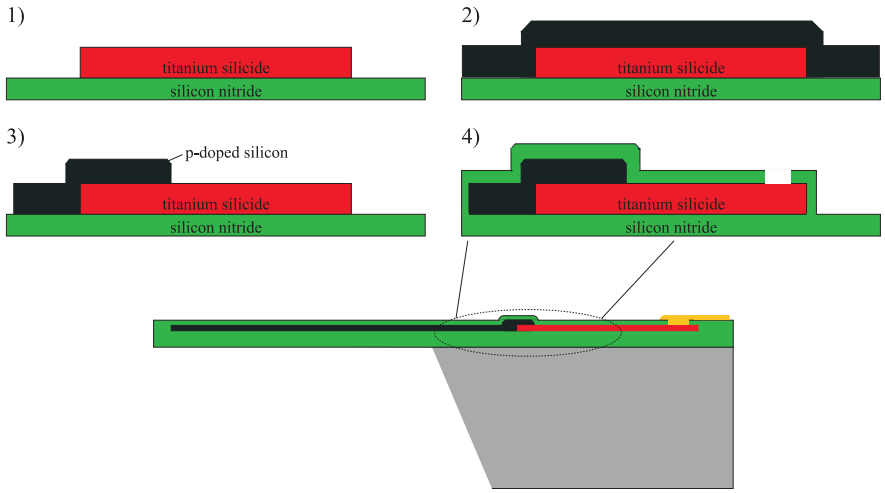


Figure 5.1: Design of cantilever sensor with titanium silicide wiring and silicon piezoresistors encapsulated in silicon nitride. 1) The titanium silicide is formed on top of the LPCVD silicon nitride that constitutes the bottom layer of the cantilever. 2) Deposition of LPCVD silicon and subsequent ion implantation. 3) Defining piezoresistors with RIE. 4) Deposition of LPCVD silicon nitride. Contact holes opened with RIE.

are encapsulated in LPCVD silicon nitride. The cantilevers are released by etching with KOH from the back of the wafer.

5.1.1 Design optimisation, the 1st generation

The optimal design with regard to the dimensions of the cantilever and piezoresistor is found by minimising the minimum detectable surface stress from page 25

$$\sigma_{s\ min} = \frac{V_{noise}}{\frac{1}{4}(\frac{\Delta R}{R}\sigma_s^{-1})V_{in}} \tag{5.1-1}$$

The model for a beam is used as a best approximation, so from table 3.1

$$\frac{\Delta R}{R} = \varepsilon_x[K_L + K_T] \tag{5.1-2}$$

where the strain $\varepsilon_x = \varepsilon_0 + \beta z$ is given in section 3.6.1.

The last parameters to determine are the gauge factors. It is not easy quantitatively to calibrate with surface stresses, and therefore the bending sensitivity as described in section 3.5 is used to determine the relation between the strain and the resistance change. In equation 3.5-7

$$\frac{\Delta R}{R}z^{-1} \propto [K_L(A - \nu B) + K_T(B - \nu A)] \tag{5.1-3}$$

the resistance change as a function of the gauge factors is described for a force working on the apex of the cantilever. The procedure is then to bend the cantilever a known distance z and record the resistance change $\Delta R/R$. With the approximation that the longitudinal part of the resistance is much larger than the transversal part ($A \gg B$) then $\Delta R/R \propto K_L - \nu K_T$. If Poisson contraction ($\varepsilon_T = -\nu\varepsilon_L$) is ignored then $\Delta R/R \propto K_L$. The values found from these tests give $K_L = 20 - 30$ depending on doping concentration and annealing treatments[25], which are in good agreement with the gauge factors for poly silicon reported in the literature[82, 83, 84]. Obermeier *et al.*[82] have tested the longitudinal and transversal gauge factors for boron doped polysilicon and their results are shown in figure 5.2. It is seen that the longitudinal gauge factor is between 20 and 30 and that, for most doping concentrations, the longitudinal gauge factor is 2-3 times larger than the transversal gauge factor. This then support the assumption that $K_L - \nu K_T \simeq K_L$.

Taking this assumption one step further it is assumed that the sensitivity to surface stress in equation 5.1-2 is given by

$$\frac{\Delta R}{R} = \varepsilon_x K_L \tag{5.1-4}$$

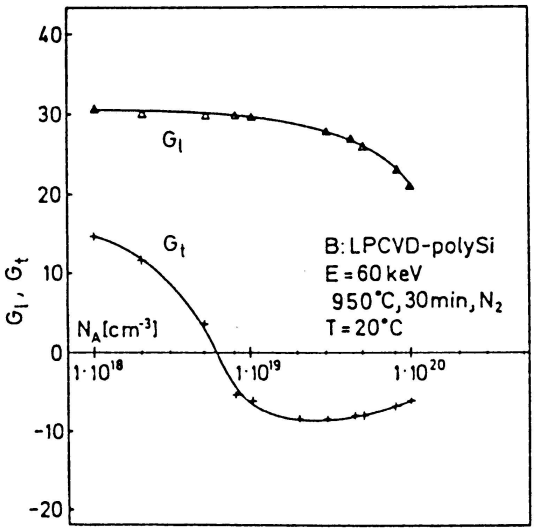


Figure 5.2: Longitudinal and transversal gauge factors for boron doped polysilicon[82].

Optimised cantilever

The fitting parameters available when minimising $\sigma_{s\ min}$ are detailed in figure 5.3. They include the thicknesses of the thin films and the dimensions of the

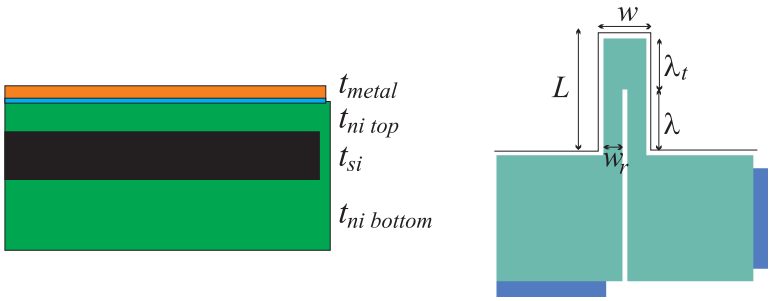


Figure 5.3: Geometry of the cantilever sensor. To the left is shown a cross section of the cantilever. The metal on top is used for immobilising biological samples. The dimensions of the cantilever and piezoresistor are shown to the right.

cantilever and resistor. Some of the dimensions are interlinked so that the width and length of the cantilever are governed by the width and length of the resistor. This is no simplification of the problem since it was shown in the theory that the strain and thus the sensitivity were not dependent on the length and width of the cantilever. The thicknesses of the metal layers on top of the cantilever are fixed. A thin gold layer is typically used for immobilising biological samples. The parameters used are given in table 5.1. This basically leaves back the six fitting

K	α	Δf	V_{in}	ϱ
30	$1.4 \cdot 10^{-3}$	1-51 Hz	5 V	$8 \cdot 10^{-3}$ Ω·cm

Material	Au	Cr	Si_3N_4	Si
E [GPa]	79	279	200	170
ρ [kg/m^3]	19231	7190	3100	2330

Table 5.1: Top: Parameters used for the optimisation. The gauge factor, the α-value[25] and the resistivity are estimated values for polysilicon with a boron dose of $2 \cdot 10^{20}$ cm^{-3}. The bandwidth of 1-51 Hz is chosen such that the low frequency 1/f noise is included.
Bottom: Young's modulus and density used for the materials.
The metal layers on top of the cantilever are chromium/gold 5 nm/40 nm. For all layers a Poisson's ratio of 0.25 is used.

parameters:

$$t_{ni\ top},\ t_{ni\ bottom},\ t_{si},\ w_r,\ \lambda \text{ and } \lambda_t.$$

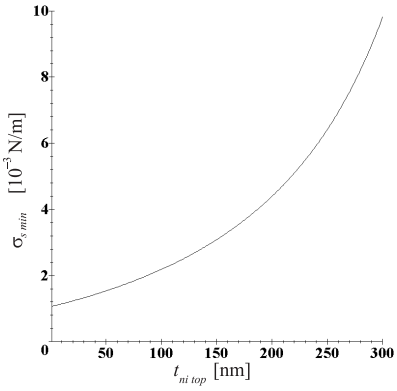
As a starting point the dimensions listed below are used:

$$t_{ni\ top}\text{=100 nm},\ t_{ni\ bottom}\text{=200 nm},\ t_{si}\text{=200 nm},$$
$$w_r\text{=20 μm},\ \lambda\text{=100 μm and } \lambda_t\text{=20 μm}.$$

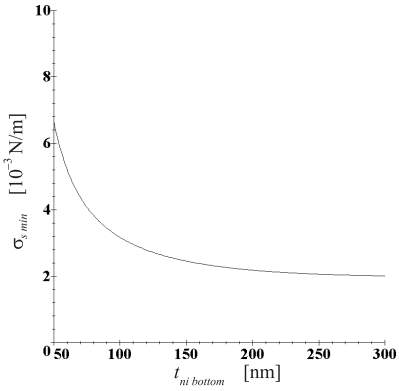
In figures 5.4, 5.5 and 5.6 the variation of $\sigma_{s\ min}$ is showed as a function of the six fitting parameters.

$\sigma_{s\ min}$ is plotted in figure 5.4(a) as a function of the thickness of the top silicon nitride layer. As could be expected from theory the thinner the layer the better the resolution. The thinner the top silicon nitride layer gets the closer the silicon resistor is placed to the surface of the cantilever, where the largest strain is. The thickness of this layer is chosen to have a thickness of 50 nm. In figure 5.4(b) $\sigma_{s\ min}$ is plotted against the thickness of the bottom silicon nitride layer. $\sigma_{s\ min}$ is decreasing with a thicker nitride layer as the distance between the resistor and the neutral plane increases. As the thickness increases this effect will eventually be counter weighted by the decreasing sensitivity as the cantilever gets stiffer.

In figure 5.5 $\sigma_{s\ min}$ is plotted as a function of the thickness and width of the silicon resistor. Both graphs show that $\sigma_{s\ min}$ falls as the dimensions of the resistor grows. This is because the 1/f noise is reduced as the number of charge carriers is increased. For t_{si} the same effect as for $t_{ni\ bottom}$ applies and the sensitivity will decrease for large thicknesses, which again will lead to a higher $\sigma_{s\ min}$. For the width $\sigma_{s\ min}$ will continue to fall as w_r grows and the width is set to 40 μm. This is 2.7 times larger than for the test structures on page 40 and is expected to decrease the spreading resistance as well as the contact resistance,



(a) $\sigma_{s\ min}$ as a function of the thickness of the top silicon nitride layer.



(b) $\sigma_{s\ min}$ as a function of the thickness of the bottom silicon nitride layer.

Figure 5.4: The minimum detectable surface stress $\sigma_{s\ min}$ plotted against fitting variables.

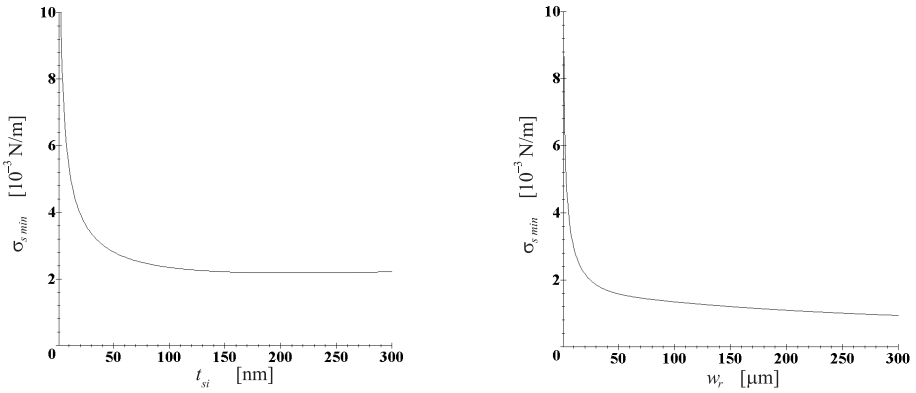
see discussion on results in table 4.6.

Figure 5.6 shows the minimal detectable stress as a function of the length of the resistor legs λ and the width λ_t of the top of the resistor. The physical difference between Johnson noise and 1/f noise can be seen in the plot of the resolution as a function of resistor length λ: The Johnson noise increases with increased resistor length whereas the 1/f noise decreases with increasing resistor length. For λ_t goes that the noise is lowered as the height grows. At the same time the resistance of the top part of the resistor falls and eventually the effect from this part of the resistor vanishes.

When optimising the parameters in an iterative process it is found that the minimum value for $\sigma_{s\ min}$ is found for λ=1.53 mm, t_{si}=150 nm and $t_{ni\ bottom}$=220 nm. λ was then set to 110 µm. A cantilever with a length of 1.5 mm would not fit into a normal micro liquid channel system, and with a spring constant of around 10^{-4} N/m it would probably be very susceptible to noise and fluctuations in the liquid flow. A new optimisation gave the same values for $t_{ni\ bottom}$ and t_{si} as the sensitivity is not changed with the length of the cantilever, increasing λ only decreases the 1/f noise. With these dimensions

$$t_{ni\ top}=50 \text{ nm}, t_{ni\ bottom}=220 \text{ nm}, t_{si}=150 \text{ nm},$$
$$w_r=40 \text{ µm}, \lambda=110 \text{ µm and } \lambda_t=40 \text{ µm}$$

the expected performance of the sensor is listed in table 5.2. The resolution is close to 1 mN/m which in principle suffices to measure hybridisation signals as for example reported by Fritz *et al.*[44].



(a) $\sigma_{s\ min}$ as a function of the thickness of the silicon piezoresistor.

(b) $\sigma_{s\ min}$ as a function of the the width of the piezoresistor.

Figure 5.5: The minimum detectable surface stress $\sigma_{s\ min}$ plotted against fitting variables.

k [N/m]	f [kHz]	$\sigma_{s\ min}$ [N/m]	$\frac{\Delta R}{R}\sigma_s^{-1}$ [(N/m)$^{-1}$]
0.11	20	$8.0 \cdot 10^{-4}$	$5.7 \cdot 10^{-4}$

Table 5.2: The calculated performance of the cantilever stress sensor.

Mask layout

The masks designed for the cantilever sensor are shown in figure 5.7.

Mask (a) defines the wiring in the polysilicon.

Mask (b) is the titanium lift-off mask for the wiring.

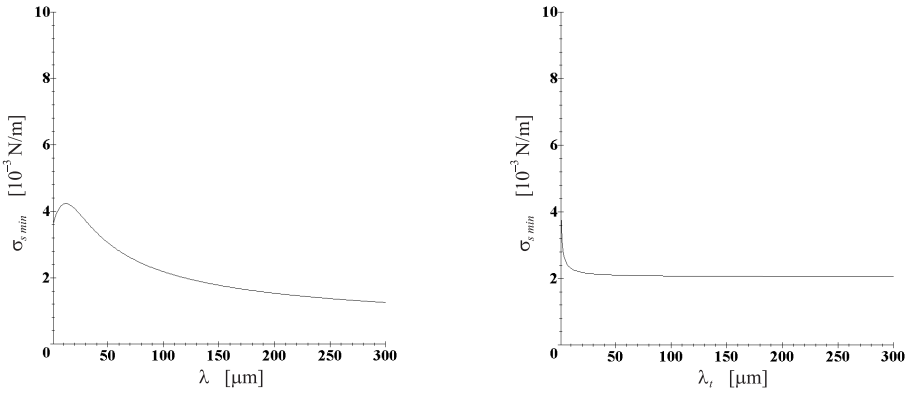
Mask (c) is a mask for implanting the top part of the resistor with a higher dopant concentration than the rest of the silicon resistor.

Mask (d) defines the silicon piezoresistors. The overlap between the silicon and the underlying titanium silicide is 300 µm×800 µm.

Mask (e) defines the contact holes and the cantilever.

Mask (f) is for patterning metal contacts on the contact holes.

Finally, mask (g) is defining the etch mask on the back of the wafer. The small 'arms' on the mask are holding the chips together in a grid when the wafer is



(a) $\sigma_{s\ min}$ as a function of the length of the legs of the piezoresistor.

(b) $\sigma_{s\ min}$ as a function of the width of the top of the piezoresistor.

Figure 5.6: The minimum detectable surface stress $\sigma_{s\ min}$ plotted against fitting variables.

etched in KOH. After the KOH etch the chips can be taken manually by breaking the arms[54].

5.1.2 Realisation of the 1st generation

The process sequence for the cantilever sensor is described here. A specific process sequence with *e.g.* baking times and process recipes is to be found in appendix B.

The processing is sketched schematically in figure 5.8. The wafers are 4" double sided polished 350 μm thick silicon wafers.

In the first step a low stress silicon rich LPCVD silicon nitride is deposited(figure a) followed by an LPCVD silicon layer for the wiring (figure b).

Next, the wiring is formed. The titanium silicide is made of 800 Å titanium deposited on top of 2200 Å amorphous silicon. The silicon is patterned with a wet etch with selectivity to the silicon nitride, which is important since this layer defines the bottom silicon nitride in the cantilever and the thickness is important with regard to the performance of the sensor (figure c). A titanium layer is patterned on top of the silicon wires with a lift-off process (figure d), and annealed in an RTA process to form the titanium silicide (figure e). Remaining titanium is etched in piranha.

For the piezoresistors an LPCVD polysilicon layer is deposited(figure f), ion im-

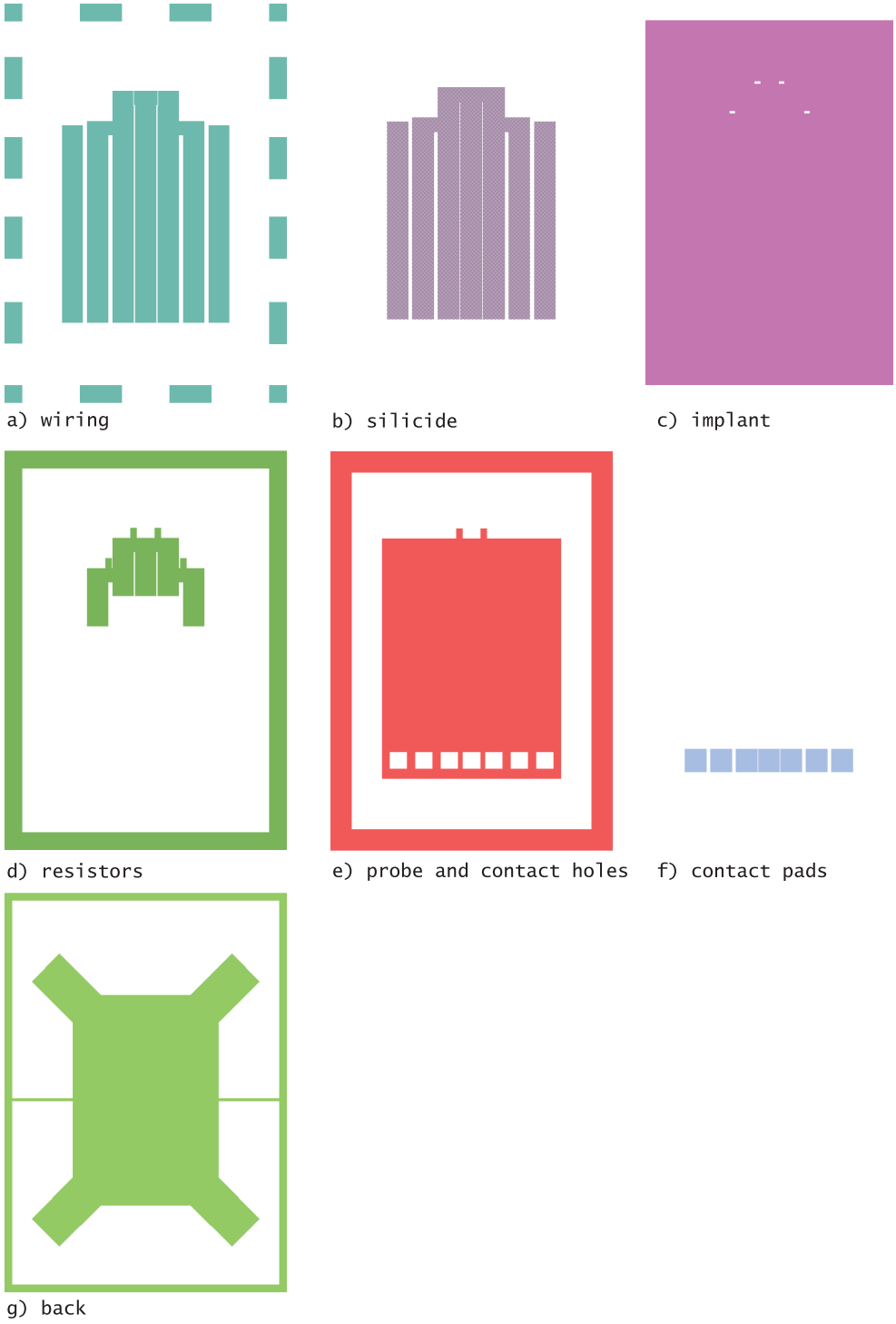


Figure 5.7: Mask set. Not depicted here is the mask for defining the metal layer on the cantilever.

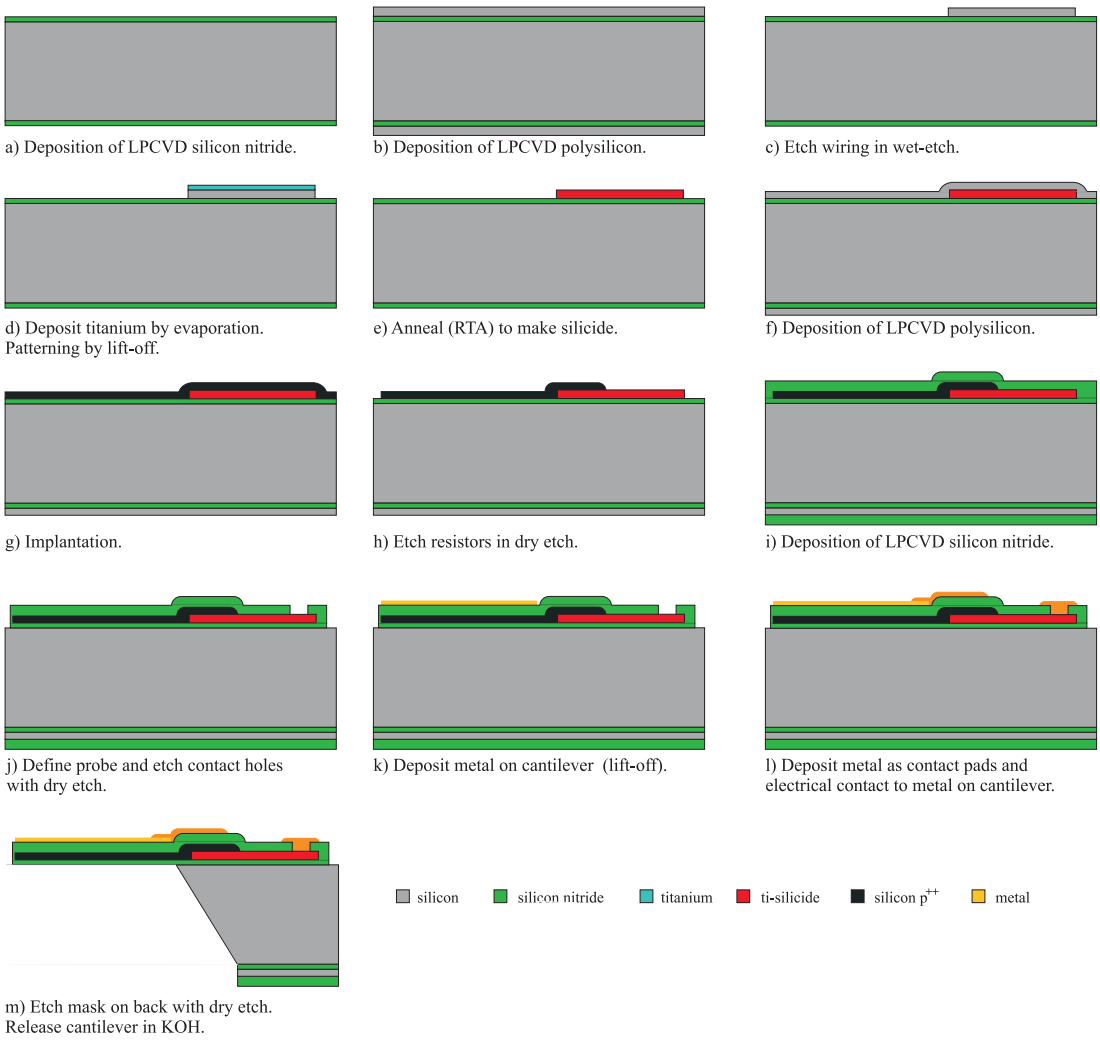


Figure 5.8: Process sequence.

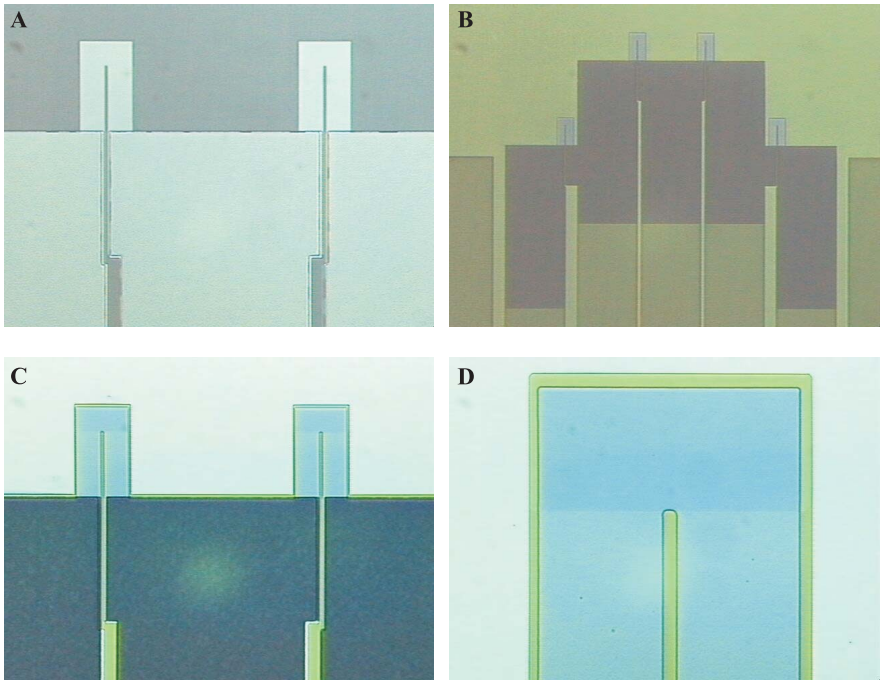


Figure 5.9: Optical images from process. A: After the definition of the resistors with RIE. B: 50 nm of silicon nitride deposited on the wafer. C: Definition of the cantilever and body of the chip with RIE. D: Zoom-in on resistor from figure C.

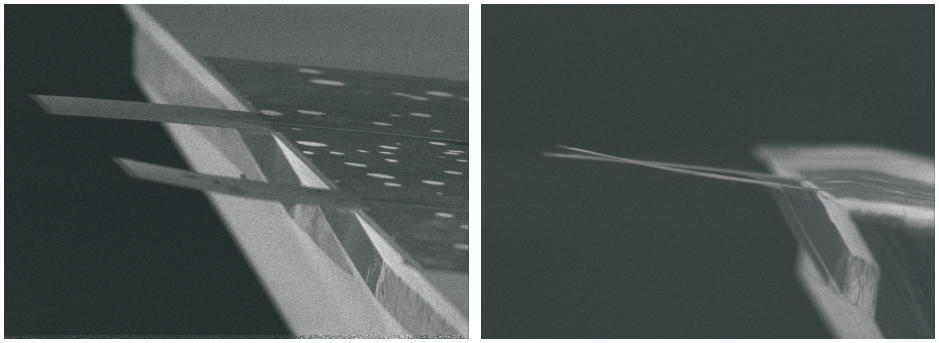


Figure 5.10: Chips after KOH etch. Left: the two cantilevers and the overlap area between titanium silicide and silicon which has been damaged visibly. Right: The cantilever with the thin Cr/Au metal layer on top bends more than the other cantilever. The length of the cantilevers is 150 µm.

planted with boron to obtain a dopant concentration of $2 \cdot 10^{20}$ cm^{-3} (figure g) and patterned in an RIE process (figure h). An optical image of the resistors after the RIE is detailed in figure 5.9A.

The whole structure is covered with low stress LPCVD silicon nitride (figure i and optical image in figure 5.9B). The activation of the boron is done in an RTA process at 900°C for 1 minute.

The cantilever and the contact holes for the wiring are made in an RIE process in a CHF_3/N_2 plasma (figure j and optical images in figure 5.9 C and D).

A 5 nm chromium/40 nm gold layer is formed on the cantilever in a lift-off process (figure k). This layer can later be used for immobilisation of specific molecules. 10 nm chromium/200 nm gold contacts are similarly patterned with lift-off (figure l).

In the last process step the cantilevers are released in KOH (figure m). The wafer is placed in a holder that protects the front of the wafer against the KOH until the wafer is etched all the way through.

5.1.3 Evaluation of the 1st generation

After the release etch in KOH, the wiring was attacked. Figure 5.10 shows pictures of the cantilevers, and it is seen on the left picture how the contact pads between silicide and silicon are damaged. In figure 5.11 it can be seen how the titanium silicide wiring is etched under the silicon nitride. It can be seen how the edges of the titanium silicide wiring (in-set lower right) are attacked. In the overlap area between the silicon and the titanium silicide it looks as if a lot of

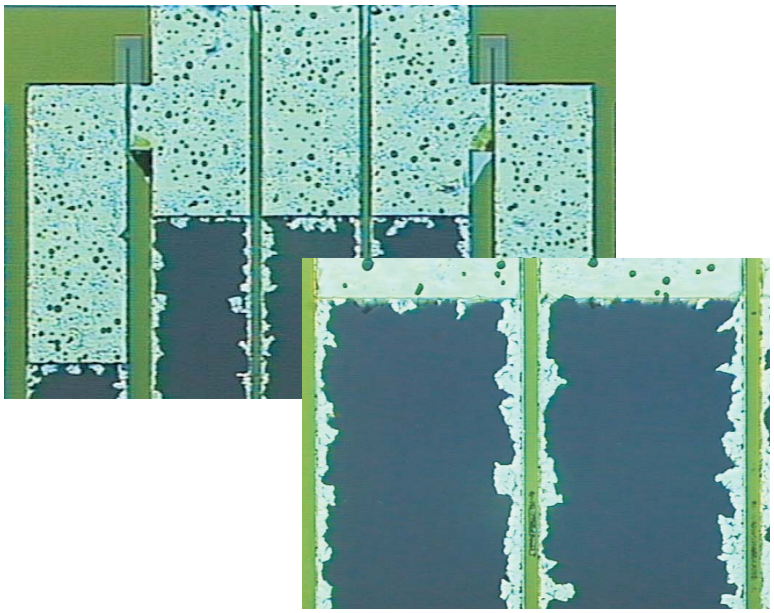


Figure 5.11: Chip after KOH etch. The wires have a width of 300 µm.

small holes are etched in the silicon. On the silicon resistors, however, no attack of the silicon is observed. This shows that the quality of the silicon nitride is good enough to stand the KOH, and it also shows that the problem lies in the combination of the titanium silicide and the silicon nitride.

For this reason it was not possible to test the sensors, and further testing was needed.

5.2 The 2nd generation

The wiring on the chips in the 1st generation failed to stand the KOH etch. The problem was localised to the sandwich of the titanium silicide wiring and the silicon nitride coating. The titanium silicide wiring and the coating hereof was therefore subject to further testing.

5.2.1 Process optimisation of coating

The titanium silicide wiring with a coating of LPCVD silicon nitride had been tested successfully in KOH during the initial process optimisation. The reason for failing on the real chip must be the heat treatment the chips are subjected to after the deposition of the silicon nitride in order to activate the dopant in the resistors. It was an RTA for 60 s at 900°C, which is the nominal temperature, so the real temperature of the top layers are probably around 1000°C. The thermal expansion coefficients of the titanium silicide (12.5 ppm/°C[85]) and the silicon nitride (3.2 ppm/°C[85]) have a large mismatch of about 9 ppm/°C as compared to the mismatch of 0.5-1 ppm/°C between silicon and silicon nitride. This mismatch in thermal expansion has probably created small cracks in the silicon nitride during the RTA activation of the boron.

Effect of RTA on coating

This hypothesis was tested on a set of wafers with titanium silicide wiring coated with either 500 Å or 1000 Å of silicon nitride. On these wafers the titanium silicide was formed in an RTA at 775°C for 60 s and then coated with silicon nitride. The wafers were cut in half and half the wafer was then annealed at 1000°C for 60 s while the other half was a reference which was not annealed. The wafers were subsequently immersed in 80°C KOH for 30 min. An example of one of the test wafers is shown in figure 5.12. The tests showed generally that the 1000 Å

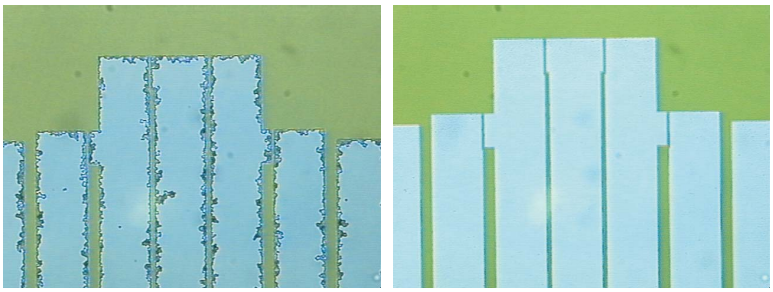


Figure 5.12: Titanium silicide coated with LPCVD silicon nitride after 30 min in 80°C KOH. Left: Annealed with RTA 1000°C/60s. Right: No extra anneal.

coating protected somewhat better than the 500 Å coating, but that the decisive

factor was whether the chips had been annealed or not. The yield of the coating was ∼100 % without the annealing and between 0 and 20 % with the annealing.

During the above tests the surface roughness of the titanium silicide wiring before the deposition of silicon nitride, after the deposition of silicon nitride and after the test in KOH was measured with a surface profilometer. They showed a peak-peak roughness of only 20 Å of the titanium silicide before the silicon nitride deposition and a peak-peak roughness of >100 Å was seen after the deposition. This could either indicate that the titanium silicide is not fully reacted to the final phase before the silicon nitride deposition or that the titanium silicide is etched by the gases in the furnace.

Two new test series emerged from this first one:

- Use a longer annealing when forming the titanium silicide to ensure that the titanium silicide formation process has stopped.
- Use a furnace annealing instead of the RTA to minimise thermal chock between titanium silicide and silicon nitride

Effect of prolonged RTA

In this test the RTA for formation of the titanium silicide of 775°C for 1 min was followed by a 2nd RTA. One set was annealed for extra 3 min at 775°C and another set was annealed an extra minute at 1000°C. After that the wafers were coated with 500 Å silicon nitride, and half a wafer was annealed at 1000°C for 1 minute before they were tested in KOH. Figure 5.13 shows an example of a chip annealed a total of 4 min at 775°C before the silicon nitride deposition. For both

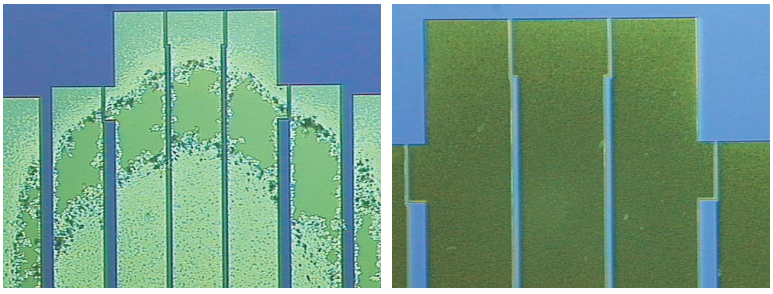


Figure 5.13: Titanium silicide coated with LPCVD silicon nitride after 30 min in 80°C KOH. Left: Annealed with RTA 1000°C/60 s. Right: No extra anneal.

RTA treatments, the extra annealing did not show any improvement in yield.

Effect of furnace annealing on coating

Wafers with titanium silicide wiring and a 500 Å silicon nitride coating were annealed at 1000°C for 20 min in a normal furnace, where the thermal shock of the titanium silicide/silicon nitride sandwich should be minimal compared to the RTA. Samples after the test in KOH are shown in figure 5.14. They show that

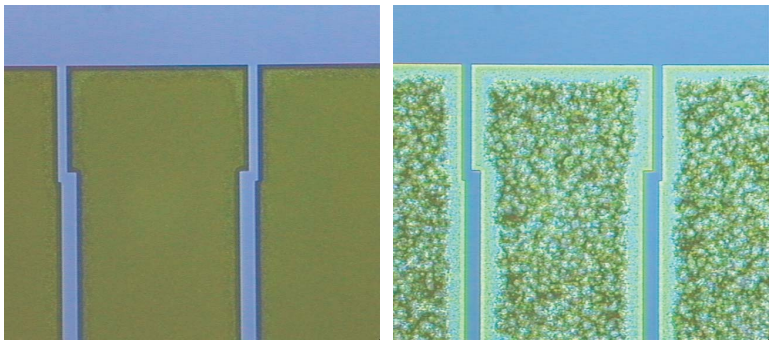


Figure 5.14: Titanium silicide coated with LPCVD silicon nitride after 30 min in 80°C KOH. Left: no extra anneal. Right: furnace anneal 1000°C/20 min.

even though the coating does not peal of as spectacularly as with the RTAs, the wires are heavily attacked under the coating, and generally the furnace anneal did not produce a yield noticeably better than the RTA.

Two-layer silicon nitride coating

Since the titanium silicide/silicon nitride stack is so sensitive to annealing treatments, is was found that a two-step coating of the wiring was necessary. This would be a thin layer of silicon nitride over the titanium silicide and silicon during the RTA activation of the dopant to prevent out-diffusion of boron and to prevent oxidation on the surfaces. After the anneal a new silicon nitride layer is deposited to close possible cracks in the coating.

This procedure was tested and optimised with a first layer of silicon nitride of 200 Å, a 1 min RTA and a final 300 Å layer of silicon nitride. This coating proved capable of withstanding the KOH test.

5.2.2 Design optimisation, the 2nd generation

For this 2nd batch it was decided to run a reference batch of chips with gold wiring that could be used as a comparison for the chips with titanium silicide wiring. In this way the sensitivity of the piezoresistors could be measured even if the titanium silicide wiring should fail. For this reason an already existing mask set was used[86]. In this mask set the contact pads and the contact holes

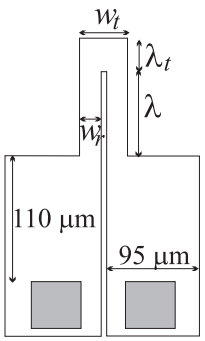


Figure 5.15: Schematic drawing of resistor and contact pads.

are placed more than 100 µm from the edge of the chip, see figure 5.15. The reasoning is that when using a metal wiring, a manual post processing coating consisting of UV glue is applied, and in order to coat the wires without coating the cantilevers, the metal wires has to be placed a distance away from the edge of the chip.

For the same reason, the only optimisation it was possible to do was on the thicknesses of the thin films in the cantilever, as the 2D geometry is fixed by the masks.

Optimised cantilever

The dimensions of the cantilever and resistors given from the masks are

$$w_r{=}20\ \mu\text{m},\ \lambda{=}110\ \mu\text{m and}\ \lambda_t{=}40\ \mu\text{m}.$$

Another resistor length of λ=80 µm is also on the mask, but the presented performance data is for the long resistor. The main differences between these masks and the masks used for the 1st generation are: (1) the width of the wires is smaller, 100 µm as compared to 300 µm, and (2) the contact area between wiring and piezoresistor is smaller, 70 µm×70 µm as compared to 300 µm×800 µm.

The parameters used for the optimisation are very similar to the ones used in the 1st generation, the only difference being a higher concentration of dopant. The parameters are listed in table 5.3. The optimisation result is also very similar to

K	α	Δf	V_{in}	ϱ
30	$1.4 \cdot 10^{-3}$	1-51 Hz	5 V	$6 \cdot 10^{-3}$ Ω·cm

Table 5.3: Parameters used for the optimisation. The resistivity is estimated for a boron dose of $3 \cdot 10^{20}$ cm^{-3}.

the previous owing to the fact that only the thickness of the cantilever determines the sensitivity of the probe:

$$t_{ni\ top}=50 \text{ nm}, t_{ni\ bottom}=211 \text{ nm and } t_{si}=147 \text{ nm}$$

The expected performance is listed in table 5.4. Notice the sensitivity $\frac{\Delta R}{R}\sigma_s^{-1}$

k [N/m]	f [kHz]	$\sigma_{s\ min}$ [N/m]	$\frac{\Delta R}{R}\sigma_s^{-1}$ [(N/m)$^{-1}$]
0.04	17	$1.1 \cdot 10^{-3}$	$4.8 \cdot 10^{-4}$

Table 5.4: The calculated performance of the cantilever stress sensor.

which is noticeably smaller than the $5.7 \cdot 10^{-4}$ (N/m)$^{-1}$ obtained for the 1st generation chips. This is due to the 'dead' series resistance in the long silicon contact wires (110 µm×95 µm) that amounts to ∼15 % of the total resistance and hence reduces the sensitivity by 15 %.

The layout for the masks can be found in appendix C.

5.2.3 Realisation of the 2nd generation

The processing is similar to the 1st batch except for the two layers of silicon nitride. The RTA activation of the boron dopant between the two silicon nitride depositions was 900°C for 1 min.

For the chips with gold wiring, the silicon was coated with 500 Å of silicon nitride and furnace annealed at 1100°C for 20 min. The process sequence for the chips with gold wiring is sketched in figure 5.16. A detailed process sequence for both processes can be found in appendix D.

5.2.4 Evaluation of the 2nd generation

In figure 5.17 chips with titanium silicide wiring are shown. The left optical picture shows the chip just before the release etch in KOH and the right SEM picture shows the released cantilevers.
In the following the chips are characterised in order to find the resistivity and gauge factor of the polysilicon. Next, the noise spectrum is measured so that the noise in a measurement can be calculated. When having measured these parameters, the sensitivity and resolution of the surface stress sensor is calculated.

The thicknesses of the thin films obtained during the processing are:

$$t_{ni\ top}=54 \text{ nm}, t_{ni\ bottom}=220 \text{ nm and } t_{si}=150 \text{ nm}$$

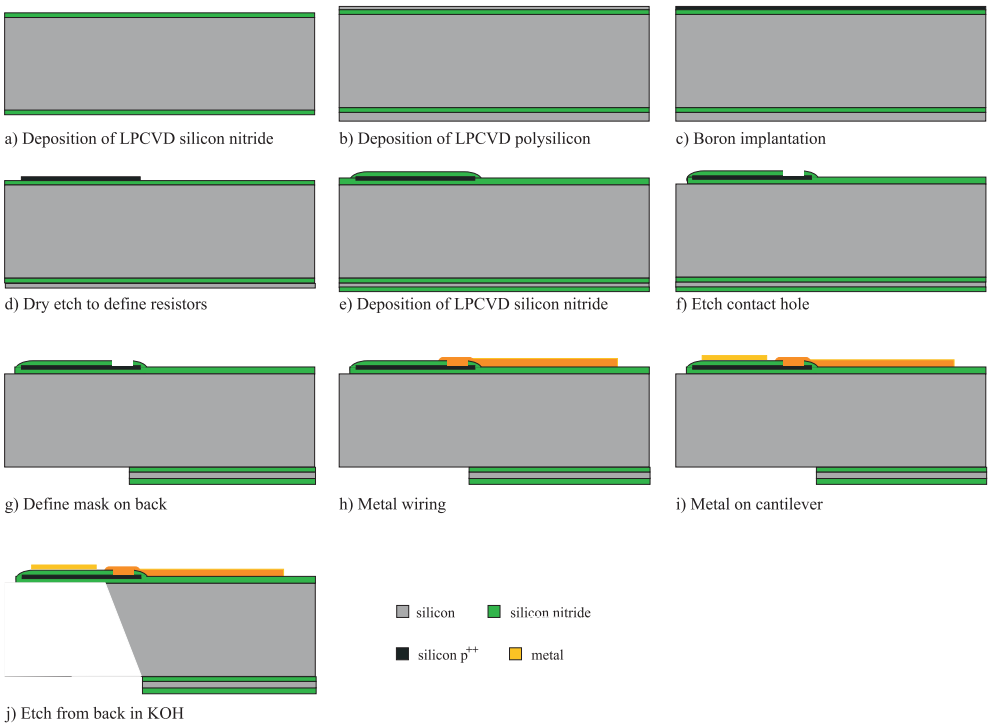


Figure 5.16: Process sequence for chips with gold wiring.

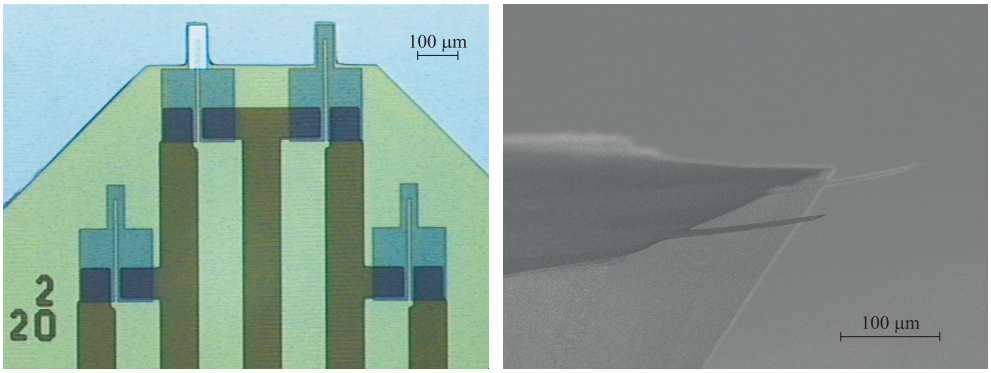


Figure 5.17: Left: Optical image of chip with titanium silicide wiring just before the KOH etch. The cantilever to the left is coated with a 40 nm gold layer. Right: SEM image of the released cantilevers after the KOH etch.

Chips with gold wiring

Resistivity

The resistance for the two different resistor lengths for the gold wire chip are plotted in figure 5.18. The resistivity of the silicon is $6.7 \cdot 10^{-3}$ Ω·cm. The total

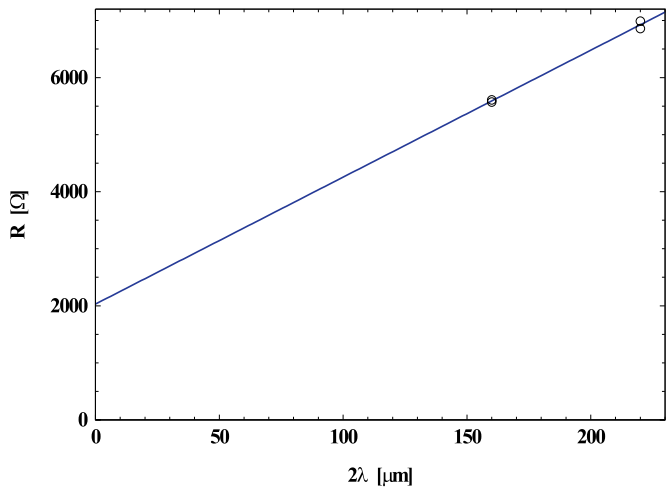


Figure 5.18: Resistance as a function of resistor length 2λ. The cut-off resistance at $2\lambda = 0$ is 2.0 kΩ. The slope is 22 Ω/ μm corresponding to a resistivity of $6.7 \cdot 10^{-3}$ Ω·cm.

measured resistance is

$$\begin{aligned} R_{total} &= R_{top} + R_{legs(2\lambda)} + R_{series} \\ &= R_{top} + \varrho\frac{2\lambda}{w_r t_{si}} + \varrho\frac{2 \cdot 110\ \mu\text{m}}{t_{si} \cdot 95\ \mu\text{m}} \end{aligned} \tag{5.2-1}$$

R_{series} is the resistance of the silicon contact wires sketched in figure 5.15. The cut-off resistance of 2.0 kΩ is R_{top}+R_{series} and with the above resistivity R_{series}=1 kΩ and hence 1 kΩ can be attributed to R_{top}, while $R_{2\lambda}$=4.9 kΩ for λ=110 μm. The reason why it is interesting to find out which resistance can be attributed to the different parts of the resistor and wiring is that the size of the passive part of the resistor, R_{series}, is influencing the sensitivity of the sensor.

Gauge factor

The gauge factor is measured as described in section 5.1.1. A sharp needle mounted on a micromanipulator contacts the apex and bends the cantilever while the resistance change of the silicon resistor is monitored. Measurements are shown in figure 5.19. From section 3.5

$$\frac{\Delta R}{R} z^{-1} \simeq \frac{k(L - \frac{\lambda}{2})d}{EI} K_L \tag{5.2-2}$$

Only the legs and the top of the resistor contributes to the sensitivity, and if these together are labelled 'active', then the slope of $1.8{\cdot}10^{-7}$ nm^{-1} found in figure 5.19

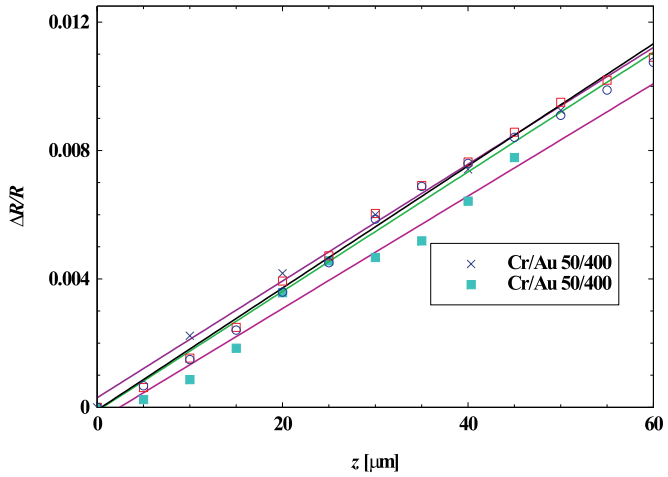


Figure 5.19: Relative resistance change as a function of bending for λ=110 µm. The graph shows four sensitivity measurements. $\frac{\Delta R}{R}z^{-1}$=1.8·10^{-7} nm^{-1} for cantilevers with a Cr/Au 5 nm/40 nm metal coating on top and 1.9·10^{-7} nm^{-1} for the cantilevers with no metal coating on top.

is actually

$$\frac{\Delta R_{active}}{R_{active}+R_{series}}z^{-1} = \frac{R_{active}}{R_{active}+R_{series}} \cdot \frac{\Delta R_{active}}{R_{active}}z^{-1} \qquad (5.2\text{-}3)$$

$\frac{R_{active}}{R_{active}+R_{series}}$ equals 0.86 so that $\frac{\Delta R}{R}z^{-1}$=1.8·10^{-7} · (0.86)$^{-1}$ nm^{-1}. Solving equation 5.2-2 now yields K_L=34.

Noise

The noise spectral density as a function of frequency is measured at different voltages, V_{in}, and plotted in figure 5.20. The curves levels at the Johnson noise spectral density of

$$\sqrt{S_J} = \sqrt{4k_BTR} \qquad [\mathrm{V}/\sqrt{\mathrm{Hz}}] \qquad (5.2\text{-}4)$$

The 1/f noise dominates at low frequencies. The 1/f voltage noise power spectral density [V^2/Hz] is given by[67]

$$S_H = \frac{\alpha V_{in}^2}{fN} \qquad (5.2\text{-}5)$$

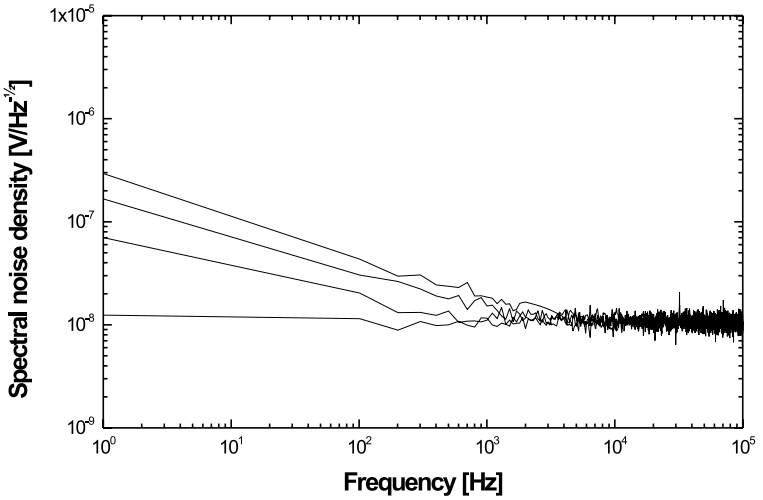


Figure 5.20: Noise spectral density as a function of frequency for a chip with λ=80 µm. The flat curve corresponds to V_{in}=0 V and from the bottom and up the next is for V_{in}=2 V, then V_{in}=4 V and V_{in}=6 V, as the 1/f noise increases with increasing voltage. The curve with V_{in}=0 V gives the spectral Johnson noise density$\simeq 10^{-8}$ V/$\sqrt{\text{Hz}}$ in accordance with $R \simeq 6$ kΩ.

and the total 1/f noise power can be written as the contributions from the top and legs of the resistor and from the series resistance as

$$\begin{aligned} S_H &= \frac{\alpha V^2}{fN}_{2\lambda} + \frac{\alpha V^2}{fN}_{top} + \frac{\alpha V^2}{fN}_{series} \\ &= \frac{\alpha}{t_{si} n} \frac{V_{in}^2}{R_{total}^2} f^{-1} \left(\frac{R_{2\lambda}^2}{2\lambda w_r} + \frac{R_{top}^2}{\lambda_t w_t} + \frac{R_{series}^2}{110\ \mu\text{m} \cdot 95\ \mu\text{m}} \right) \end{aligned} \tag{5.2-6}$$

where n is the dopant concentration in the silicon. The 1/f voltage noise density $\sqrt{S_H}$ at $f = 1$ Hz is found from figure 5.20 and plotted in figure 5.21 as a function of V_{in}. $\sqrt{S_H f}$ in figure 5.21 gives the 1/f voltage noise V_H through

$$\begin{aligned} S_H &= \frac{\text{C}(V_{in})^2}{f} \\ &\Downarrow \\ V_H^2 &= \int_{f_{min}}^{f_{max}} S_H \text{d}f = \text{C}(V_{in})^2 \ln\left(\frac{f_{max}}{f_{min}}\right) \end{aligned} \tag{5.2-7}$$

where $\sqrt{S_H f}$=C(V_{in}) is the value extracted from figure 5.21.

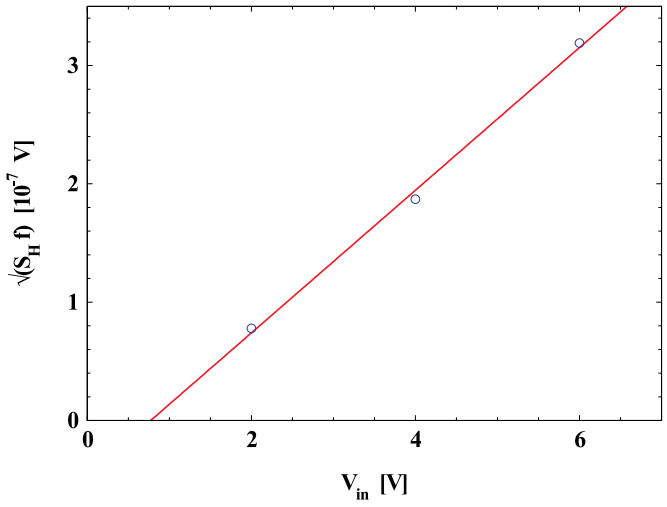


Figure 5.21: $\sqrt{S_H f}$ for f=1 Hz plotted against applied voltage. The curve gives an approximate value for the 1/f noise for applied voltages in the range between 2 V and 6 V. According to theory the 1/f noise is zero at 0 V, which is also seen in the previous figure for V_{in}=0 V.

Knowing the relation between 1/f noise $\sqrt{S_H}$ and V_{in}, equation 5.2-6 can be solved for α: $\sqrt{S_H f}$=$2.55 \cdot 10^{-7}$ V for V_{in}=5 V and f=1 Hz (from figure 5.21), which yields α=$9.2 \cdot 10^{-4}$. From $\sqrt{S_H f}$=$2.55 \cdot 10^{-7}$ V it is also found that the 1/f voltage noise, V_H, from 1-51 Hz is 0.5 μV. As a comparison the Johnson voltage noise is $\sqrt{4k_B T R \Delta f}$ = 0.08 μV, showing how 1/f noise is the dominating noise source.

Performance data

With the measured material parameters the performance can be calculated again and the results are listed in table 5.5. The calculated values are close to the

k [N/m]	f [kHz]	$\sigma_{s\ min}$ [N/m]	$\frac{\Delta R}{R}\sigma_s^{-1}$ [(N/m)$^{-1}$]
0.06	20	$8.7 \cdot 10^{-4}$	$4.7 \cdot 10^{-4}$

Table 5.5: The calculated performance of the cantilever stress sensor with the measured thin film thicknesses $t_{ni\ top}$=54 nm, $t_{ni\ bottom}$=220 nm and t_{si}=150 nm, and with ϱ=$6.7 \cdot 10^{-3}$ Ω·cm, K=30 and α=$9.2 \cdot 10^{-4}$.

expected values found in the optimisation. The calculated resolution $\sigma_{s\ min}$ is somewhat lower because the 1/f noise of the silicon is lower than expected.

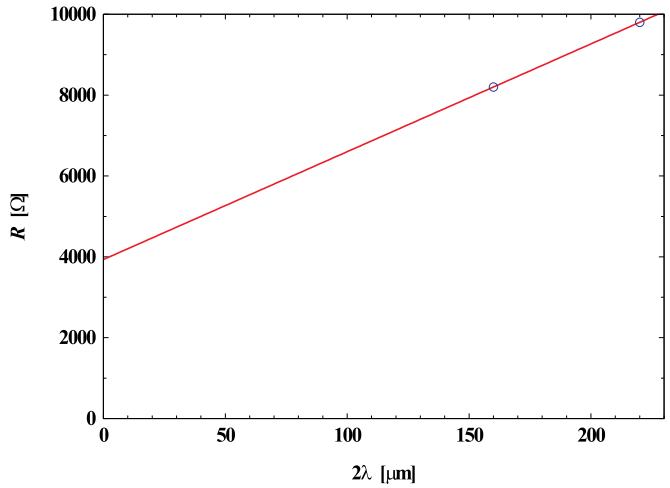


Figure 5.22: Resistance as a function of resistor length 2λ. The cut-off resistance at $2\lambda = 0$ is 3.9 kΩ. The slope is 26.7 Ω/ μm corresponding to a resistivity of $8.0 \cdot 10^{-3}$ Ω·cm.

Titanium silicide wiring chips

Resistivity

The resistance versus resistor length 2λ in figure 5.22 gives a resistivity for the silicon of $8.0 \cdot 10^{-3}$ Ω·cm. The 'dead' resistance is 3.9 kΩ. The series resistance of the silicon wiring can be calculated and it accounts for 1.2 kΩ of the 3.9 kΩ. The last 2.7 kΩ must be attributed to the resistance of the top part of the resistor, the spreading resistance at the contacts and the contact resistance between the titanium silicide and the silicon. It is most reasonable to assume that the resistance of the top part of the resistor scales with the resistivity. The resistivity is 19 % higher than for the chips with gold wiring, where R_{top} was measured at 1 kΩ. With R_{top} now estimated at 1.2 kΩ, the contact resistance and spreading resistance is then 1.5 kΩ. This indicates that in order to get a lower series resistance the high annealing temperature and time used for the chips with gold wiring is needed.

Gauge factor

The measurement for the gauge factor is shown in figure 5.23. The effective sensitivity is found to $\frac{\Delta R}{R} z^{-1}$=1.3·$10^{-7}$ nm^{-1}. Following the discussion on page 63, the sensitivity of the active resistor is $\frac{R_{total}}{R_{active}}$=1.39 times larger, giving a gauge factor of 25.

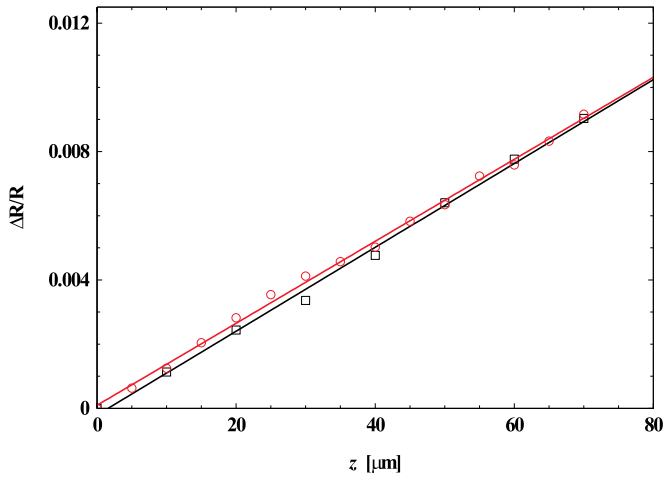


Figure 5.23: Relative resistance change as a function of bending for λ=110 μm. The graph shows two measurements. $\frac{\Delta R}{R}z^{-1}$=1.3·10^{-7} nm^{-1}.

Noise

The voltage noise spectrum is plotted to the left in figure 5.24. By comparison with the measurements on the chips with gold wiring, it is seen that the 1/f noise is higher. The 1/f noise vanishes below 5 kHz for the gold wiring chips whereas it vanishes between 50 and 100 kHz for the silicide wiring chips. In the plot of the 1/f voltage noise $\sqrt{S_H f}$ in the righthand graph in figure 5.24, it can be found that $\sqrt{S_H f}$=22·10^{-7} V at an input voltage of 5 V. From this follows from equation 5.2-7 that the 1/f noise from 1-51 Hz is 4.4 μV at V_{in}=5 V. From equation 5.2-6, an alpha value of 8.3·10^{-2} is found, which is 90 times higher than for the gold wiring chips.

The difference in α values between the two batches must be due to the different annealings of the silicon resistors. The 'gold batch' resistors were annealed at 1100°C/20 min and the 'silicide batch' at 900°C/1 min to minimise diffusion of boron. In accordance with this finding, it has been reported previously by Vandamme *et al.*[68] how annealing treatments can reduce α.

Performance data

The data for the surface stress sensor are listed in table 5.6. When compared to the chip with gold wiring, the sensitivity is 30 % lower because of the larger series resistance on the silicon/titanium silicide chips. The minimum detectable surface stress, on the other hand, is more than an order of magnitude higher, caused mainly by the very high 1/f noise which goes with $\sqrt{\alpha}$.

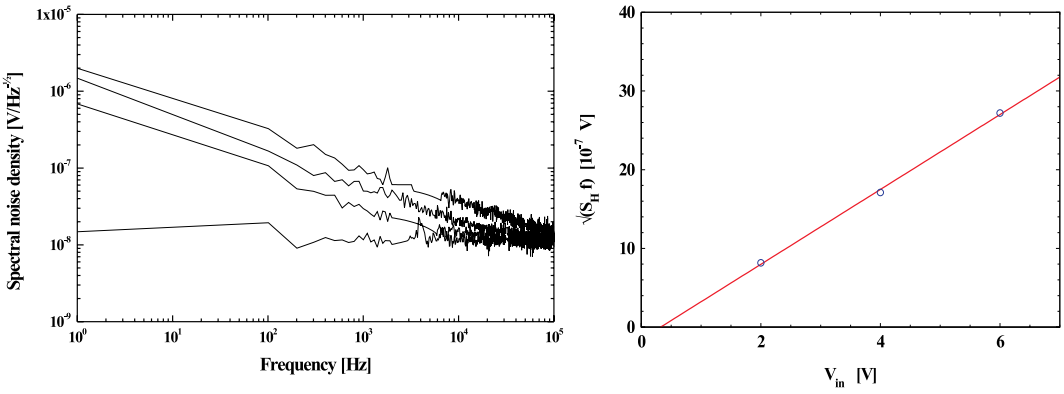


Figure 5.24: Left: Voltage noise spectrum (λ=80 µm) as a function of frequency. From bottom to top: V_{in}=0 V, 2 V, 4 V, and 6 V. Right: $\sqrt{S_H f}$ for f=1 Hz plotted against applied voltage. The curve gives an approximate value for the 1/f noise for applied voltages in the range between 2 V and 6 V. $\sqrt{S_H f}$=22·10^{-7} V for V_{in}=5 V.

k [N/m]	f [kHz]	$\sigma_{s\ min}$ [N/m]	$\frac{\Delta R}{R}\sigma_s^{-1}$ [(N/m)$^{-1}$]
0.06	20	$1.0 \cdot 10^{-2}$	$3.3 \cdot 10^{-4}$

Table 5.6: The calculated performance of the cantilever stress sensor with the measured thin film thicknesses $t_{ni\ top}$=54 nm, $t_{ni\ bottom}$=220 nm and t_{si}=150 nm, and with ϱ=8.0 · 10^{-3} Ω·cm, K=25 and α=8.3 · 10^{-2}.

Initial testing of sensor

The sensor has been operated in a liquid cell where the front part of the chip with the cantilevers is submersed. The wirebonding to the on-chip wiring is not in contact with the liquid, as sketched in figure 5.25. A first test was to etch away the 40 nm gold layer on the measurement cantilever. This measurement is shown in figure 5.26. The gold is etched with aqua regia. With the expected surface stress sensitivity of the sensor, the stress in the gold film is estimated at 30 MPa tensile stress, which is a reasonable value.

A test with the immobilisation of single stranded DNA (ssDNA) was performed in the same liquid cell. The immobilisation signal can be seen in figure 5.27. The immobilisation signal corresponds to a surface stress change of ∼0.1 N/m.

5.2.5 Conclusions on the 2nd generation

Two different batches of sensors with polysilicon piezoresistors were made and tested: one with gold wiring where the polysilicon was annealed by a standard

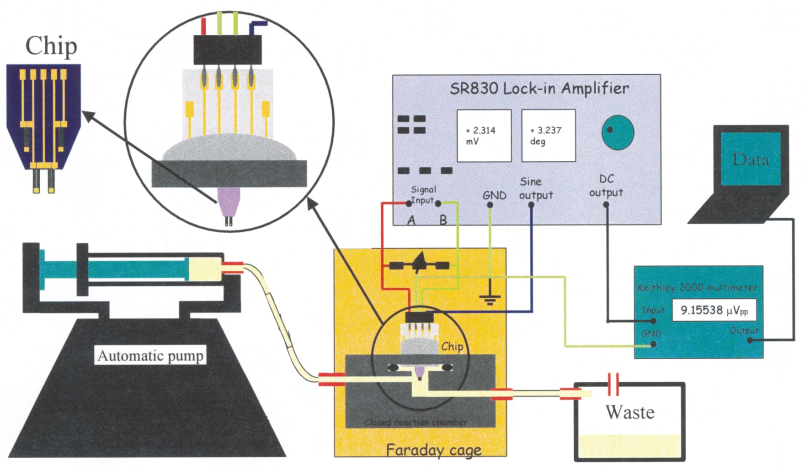


Figure 5.25: Setup for measurement in liquid cell. Drawing is taken from[87]. At the upper left the chip is mounted on a ceramic board. In the middle the chip is inserted into the liquid cell.

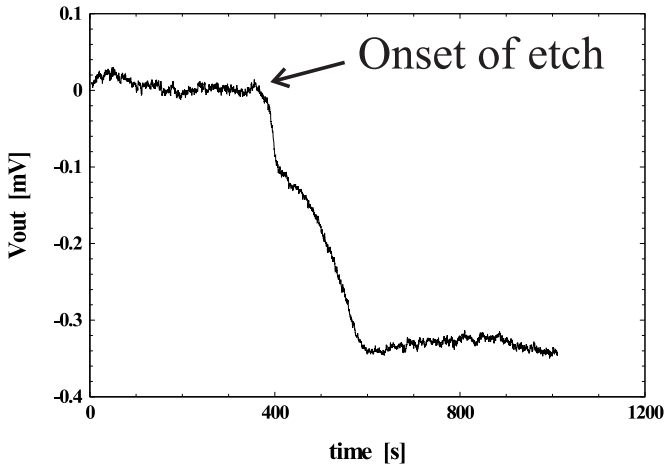


Figure 5.26: Etching of a 40 nm gold layer on the measurement cantilever. The gold is etched with aqua regia. The signal corresponds to the release of a 30 MPa tensile stress in the gold film.

furnace annealing at 1100°C, and one with titanium silicide wiring where the polysilicon was annealed by RTA at 900°C. In terms of activation of the boron dopant, they showed similar results with the furnace annealed resistors having a resistivity which is lower by 16 %. A large series resistance on the titanium silicide/silicon chips made the sensitivity 30 % lower for the RTA processed sensor. However, the masks used for this 2nd generation chips were not optimised for silicide wiring, and have a contact area between the wiring and the resistor

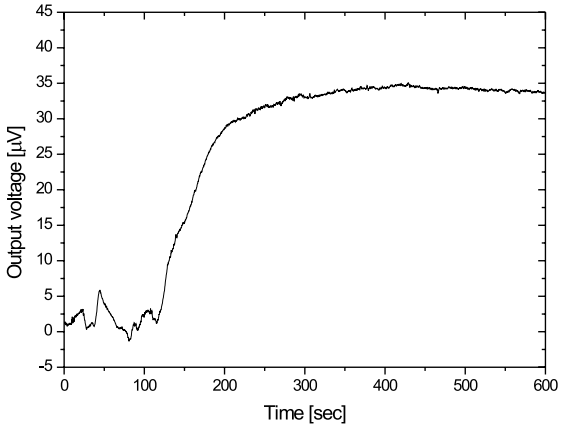


Figure 5.27: Immobilisation of ssDNA on the gold layer on the measurement cantilever. A 10 µM solution is pumped through the cell.

that is only 2 % of the contact area in the masks used for the 1st generation chips.

In terms of noise, the 1/f noise in the furnace annealed silicon is about 9 times better, which indicates the formation of larger crystals with the furnace annealing than with the RTA. The resolution is therefore an order of magnitude lower for the furnace annealed resistors. The RTA was chosen in order to minimise the diffusion of the dopant, since tests had revealed that high annealing temperatures and long annealing times give a high contact resistance between the silicon and the titanium silicide. For the same reason, the titanium silicide is formed before the silicon resistors. The results from these 2nd batch show that in order to get a low noise and a high resolution, it is necessary to do a furnace annealing of the resistors. As it furthermore was found for the 1st generation that the titanium silicide/silicon nitride combination could not stand high annealing temperatures, the conclusion is that the annealing of the resistors has to be done before the formation of the titanium silicide wiring.

The chips have also been tested in a wet biochemical measurement setup, and the immobilisation of ssDNA was detected.

5.3 The 3rd generation

In the 3rd generation the silicon resistors are defined, implanted and annealed prior to the formation of the titanium silicide wiring. This will make it possible to make a high temperature furnace annealing of the resistors before the contacts between the wiring and the resistors are made.

This also adds the simplification to the process that only one silicon nitride deposition over the titanium silicide wiring is needed.

5.3.1 Design optimisation, the 3rd generation

The optimised dimensions are the same as for the 1st generation chips.

Mask layout

Because of the changed process sequence three new masks are introduced.

The silicon resistors are coated with silicon nitride before the silicon for the silicide wiring is deposited, so an extra mask to open a contact area to the resistors is introduced.

Two other masks are introduced because the definition of the probe and the contact holes to the silicide, mask (e) in figure 5.7, are done in two different process steps in order to minimise the etch on the silicide contact pads (see subfigures (k) and (l) in the the process sequence).

The rest of the mask set from the 1st generation is reused.

5.3.2 Realisation of 3rd generation

The process sequence is illustrated in figure 5.28. The processing is described in detail in appendix E. The process steps pointed out below are those that differs from the previous process sequence.

In step (d) the wafers are annealed at 1100°C for 30 min.

In step (h) the silicon wiring is etched in an RIE process and some of the silicon nitride on top of the resistor is etched. Therefore 400 Å of silicon nitride is deposited in step (g) - of which some is etched in step (h) - and in step (k) 500 Å of silicon nitride is deposited to cover both the wiring and the resistors. These thicknesses of the silicon nitride layers were chosen to make the process robust, *i.e.* not so sensitive to a very precise etch stop, but the price is that the sensors

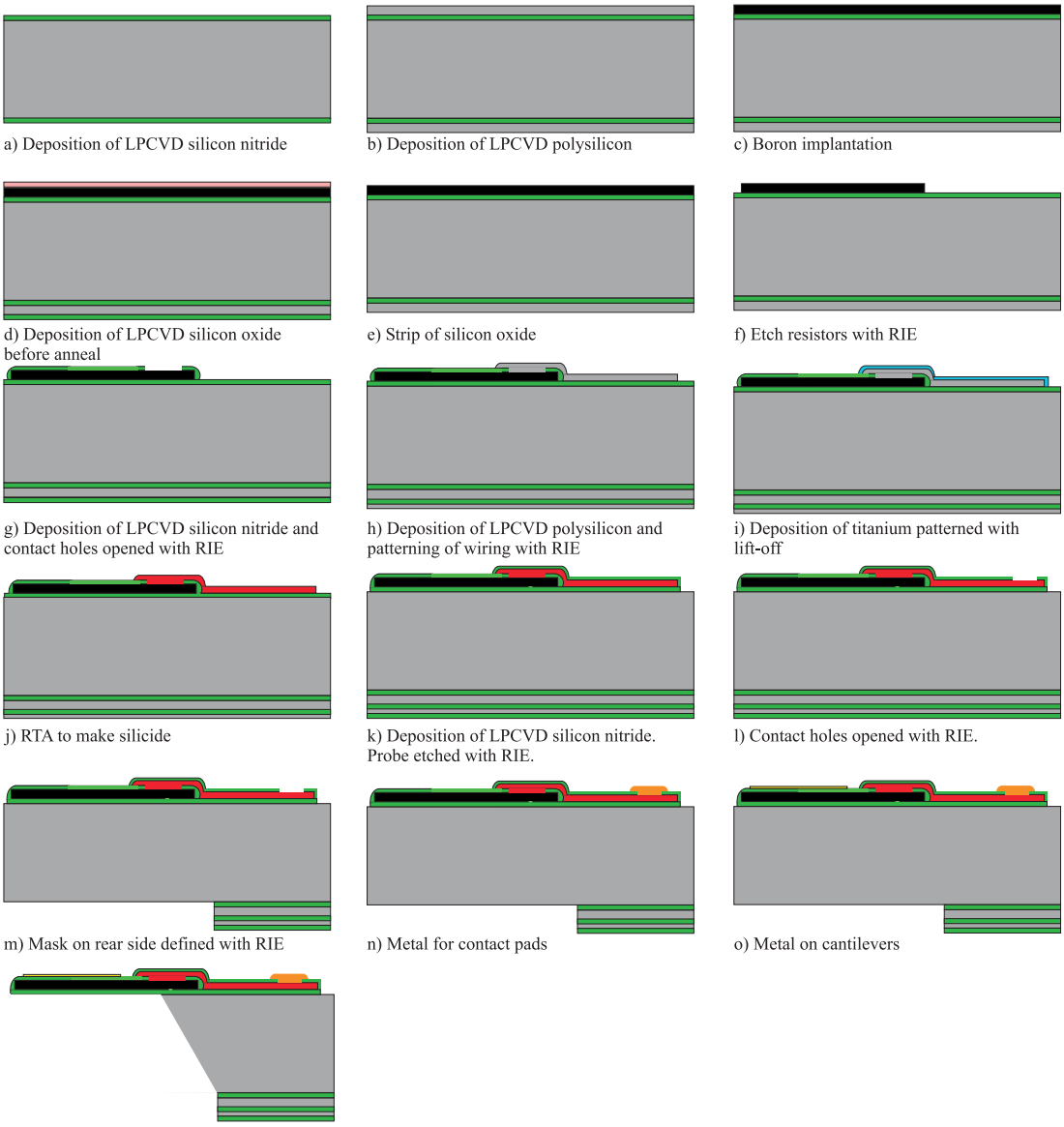


Figure 5.28: Process sequence

most likely end up with a top silicon nitride layer of thickness 7-900 Å, instead of the 500 Å aimed for in the previous processes, at the expense of lost sensitivity.

5.3.3 Evaluation of 3rd generation

The obtained thicknesses of the thin films are:

$$t_{ni\ top}=80 \text{ nm}, \ t_{ni\ bottom}=220 \text{ nm and } t_{si}=150 \text{ nm}.$$

A SEM picture of the finished chip is detailed in figure 5.29.

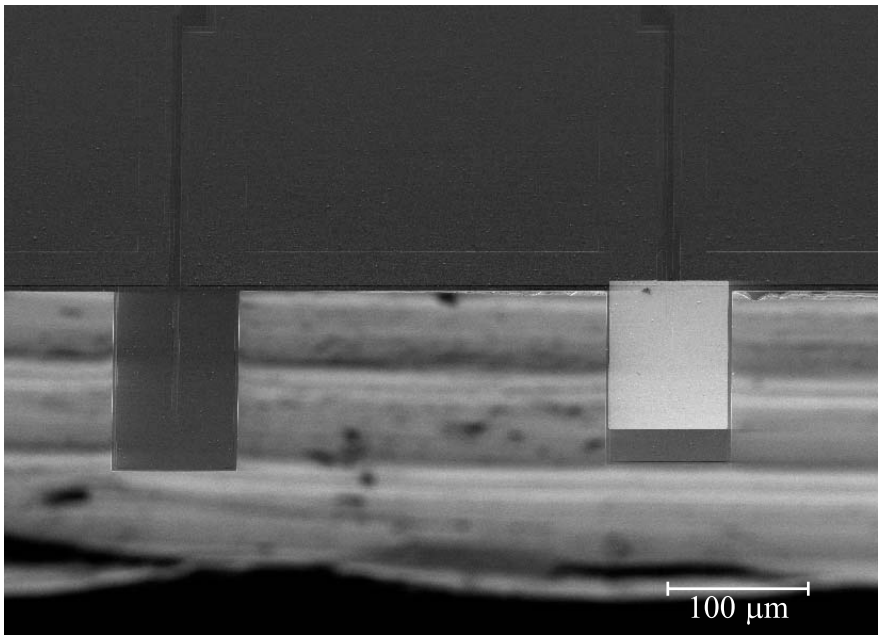


Figure 5.29: SEM picture showing the chip from the front. The cantilever to the right is coated with a chromium/gold layer.

Resistivity

As there is only one length of resistor, the resistivity can only be determined approximately.

First it is assumed that the contact resistance is negligible. Even with the contact resistances found in table 4.1.2 on page 40 of around 200 Ω, this resistance amounts to less than 5 % of the total resistance of 4.7 kΩ, and with the wider resistor legs compared to the test structures, the contact resistance is probably considerably lower.

For the top part of the resistor it is assumed that it has a resistance of twice that of the nominal resistance, $\varrho\frac{w_t}{\lambda_t t_{si}}$, which was the finding for the 2nd generation chips. R_{total} is measured at 4.7 kΩ and the resistivity follows from

$$\varrho = R_{total}\left(2\frac{w_t}{\lambda_t t} + \frac{2\lambda}{w_r t}\right)^{-1} = 7.4 \cdot 10^{-3}\ \Omega \cdot \mathrm{cm} \qquad (5.3\text{-}1)$$

This is very close to what was expected (it was $6.7 \cdot 10^{-3}\ \Omega \cdot$ cm for the furnace annealed resistors in the 2nd generation). This indicates that the contact resistance indeed is small compared to the resistance of the piezoresistor.

k [N/m]	f [kHz]	$\sigma_{s\ min}$ [N/m]	$\frac{\Delta R}{R}\sigma_s^{-1}$ [(N/m)$^{-1}$]
0.14	23	$8.8 \cdot 10^{-4}$	$4.6 \cdot 10^{-4}$

Table 5.7: The calculated performance of the cantilever stress sensor with the thin film thicknesses: $t_{ni\ top}$=80 nm, $t_{ni\ bottom}$=220 nm and t_{si}=150 nm, and with ϱ=7.4 $\cdot$ 10^{-3} Ω·cm and K=30. α=$9.2 \cdot 10^{-4}$ is assumed on the basis of the finding for the furnace annealed resistors for the 2nd generation sensors.

Gauge factor

Three different measurements of the bending sensitivity are plotted in figure 5.30. In average the sensitivities gives a gauge factor of 30, which is what was expected.

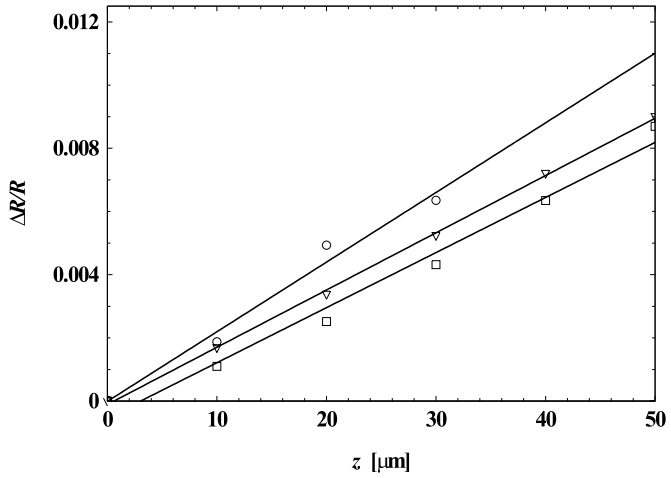


Figure 5.30: Relative resistance change as a function of bending(λ=110 μm). The measurements on three cantilevers are plotted. $\frac{\Delta R}{R}z^{-1}$=2.20·10^{-7} nm^{-1}, 1.81·10^{-7} nm^{-1}, and 1.74·10^{-7} nm^{-1}, which corresponds to an effective gauge factor of 30.

Performance data

The performance data are almost identical to those for the 2nd generation chips with gold wiring. For details see table 5.7.

5.3.4 Conclusions on 3rd generation

For the 3rd generation, the main results are that the silicide wiring is totally encapsulated in silicon nitride, and that the contact resistance between the silicon resistors and the silicide wiring is still small, as it was when the titanium silicide was formed prior to the piezoresistors.

5.4 Summary

Through three generations of chips, the practical problems of encapsulating the combined titanium silicide wiring and the boron doped silicon resistors were discovered and solved in an iterative working process. The problems included cracking during annealing of the silicon nitride covering the titanium silicide due to the thermal expansion coefficient mismatch between the two materials. As, moreover, it was shown that the polysilicon resistors needed a high temperature furnace annealing to minimise the 1/f noise, it was decided to structure and anneal the piezoresistors before the formation of the silicide wiring. Though it is suspected that diffusion of boron to the interface between the titanium silicide and the silicon resistor causes a high contact resistance, it was shown with the 3rd generation chips that with the two-layer silicon/silicide interface process, the contact resistance is insignificant. The resistors and the silicide wires proved to be fully encapsulated in the silicon nitride.

Chapter 6

SOI surface stress sensor

In this chapter the design and making of a cantilever surface stress sensor made on a silicon on insulator (SOI) substrate are described. The objective is to make the piezoresistor of single crystalline silicon, which has a higher gauge factor and a lower 1/f noise than polysilicon. The alpha value in Hooge's model for the 1/f noise is typically 3 orders of magnitude higher for polysilicon and amorphous silicon[88, 89, 25] than for single crystalline silicon[68, 25, 90]. The challenge, and the reason for not doing this from the beginning, is that it is technologically much more difficult to make a fully encapsulated piezoresistor on the SOI substrate.

Cantilevers on SOI wafers for the use in AFM were first realised in 1991 by Tortonese *et al.*[9] in Quate's group at Stanford. In the Micro Structures & Sensors Laboratory at Stanford and at IBM's Almaden Research Center, cantilevers for use in read/write applications with piezoresistors made on SOI substrates have been made, see *e.g.* Chui *et al.*[91] and Ried *et al.*[92]. Linnemann *et al.*[18] presented in 1995 an AFM cantilever made on an SOI substrate with a Wheatstone bridge placed on the cantilever. A common thing for these cantilevers has been that they are only operated in air and feature no encapsulation to make a dielectric shielding, let alone to protect them in liquid.

6.1 Design of SOI sensor

As for the sensor with polycrystalline silicon, the goal is to encapsulate the resistor in silicon nitride. Several ways to achieve this can be envisioned and three suggestions are shown in figures 6.1 A, B and C. The general problem is how to make the electrical contact pads, as any metallisation in general has to be made after a high temperature process like the deposition of LPCVD silicon nitride.

In A the cantilever is released by etching anisotropically from the front of the wafer to a depth of for example 50 μm down in the bulk silicon. This is followed

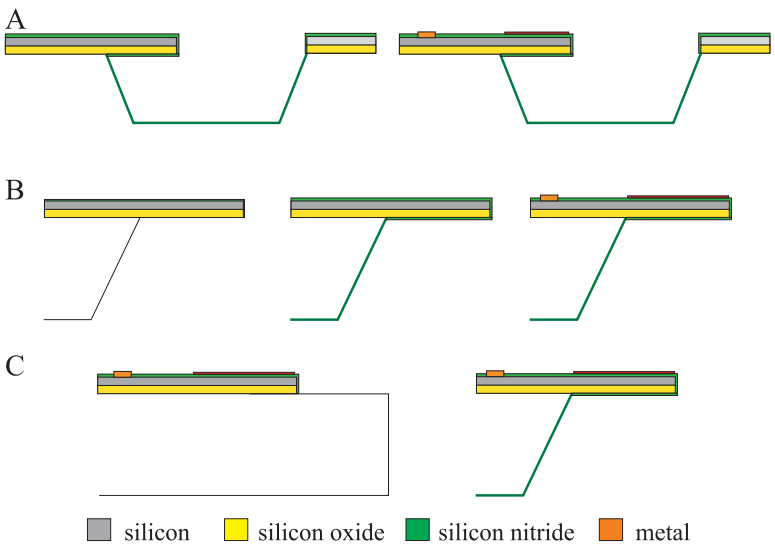


Figure 6.1: Encapsulated cantilevers on SOI substrate.
Process A: KOH etch from the front. Spinning of resist is possible after the freestanding cantilever is encapsulated in LPCVD silicon nitride.
Process B: The cantilever is encapsulated in LPCVD silicon nitride. Normal resist spinning is not possible.
Process C: Contact metallisation and metal deposition on the cantilever is done before the release etch in KOH. The bottom side of the cantilever is then coated with PECVD silicon nitride.

by an LPCVD deposition of silicon nitride. This process will make it possible to spin resist on the wafer, after the nitride deposition, in order to define the metal wiring.

The processes in B and C include a KOH etch from the back all the way through the wafer. After the KOH etch it is therefore not possible to spin resist on the wafer.

In B the cantilever is coated in LPCVD silicon nitride and the metal contacts can only be made by some kind of shadow masking or spray coated resist, since it is not possible to spin resist on the wafer after the KOH etch. The advantage is that all of the structure is coated with LPCVD silicon nitride, but shadow masking will in general be a tedious and not very precise process and spray coating equipment is not available at MIC.

In C the top of the resistor is coated with LPCVD silicon nitride, and the metal contacts and for example a metal layer on the cantilever are formed prior to the KOH etch. After the release etch, a PECVD silicon nitride is deposited on the back of the cantilever. The PECVD process is a low temperature process and is

	$[10^{-11}$ Pa$^{-1}]$		
	π_{11}	π_{12}	π_{44}
p-type	6.6	-1.1	138.1
n-type	-102.2	53.4	-13.6

Table 6.1: Piezoresistive coefficients for (100) silicon. p-type: 7.8 Ω·cm, n-type: 11.7 Ω·cm[93].

only coating one side of the wafer, and therefore the metallisation can be made before the deposition. The disadvantage of this process can be the poor step coverage and the lower quality film normally obtained with PECVD compared to LPCVD.

A process like the one sketched in A was chosen because the resistor will be coated with LPCVD silicon nitride as the previous polysilicon sensors, and because a wafer scale lithography patterning of the metal contacts is possible.

6.2 Design optimisation

For single crystalline silicon with its few defects, the piezoresistive properties are well documented[93, 94], and tabulated values for the piezoresistive coefficients together with the observations from section 3.3 are the basis for designing the cantilever sensor on the SOI substrate.

6.2.1 Single crystalline piezoresistor

In table 3.1 on page 22 the sensitivity for a cantilever beam, case C, and a cantilever plate, case D, with in-plane isotropic stress is found:

Beam: σ_x=σ_y and ε_x=ε_y (Case C)

$$\frac{\Delta R}{R} = \varepsilon_x(K_L + K_T)$$

Plate: ε_y=0 $\Rightarrow$ σ_y=$\nu\sigma_x$ (Case D)

$$\frac{\Delta R}{R} = \varepsilon_x(AK_L + BK_T)$$

In table 6.1 the piezoresistive coefficients for (100) silicon are listed. From these the longitudinal and the transversal piezoresistive coefficients along [110] directions are found and listed in table 6.2. These are the interesting directions since the cantilevers are fabricated on (100) wafers and released with anisotropic etching with the cantilever placed along the [110] direction. The gauge factors are

	[10^{-11} Pa^{-1}]			
	π_L	π_T	K_L	K_T
p-type	72	-66	122	-112
n-type	-31	-18	-52	-30

Table 6.2: Longitudinal and transversal piezoresistive coefficients for the [110] directions on (100) silicon.
$\pi_L = \frac{1}{2}(\pi_{11} + \pi_{12} + \pi_{44})$ and $\pi_T = \frac{1}{2}(\pi_{11} + \pi_{12} - \pi_{44})$.
$K = \pi E$, E_{110}=170 GPa.

calculated with a Young's modulus of 170 GPa. The gauge factor is dependent on both temperature and dopant concentration and this is illustrated from the work of Kanda[95] in figure 6.2. The piezoresistive coefficients in tables 6.1 and 6.2 are room temperature values for a low doping concentration, where the maximum piezoresistive values are obtained. The model by Kanda predicts the piezoresistive coefficient as a function of higher doping levels and as a function of temperature. Kanda calculates a pre-factor $P(N,T)$, which is plotted in the graphs in figure 6.2, which gives the piezoresistive coefficient for varying doping levels N and temperatures T as a function of the piezoresistive coefficients found at low doping levels and room temperature so that

$$\pi(N,T) = P(N,T) \cdot \pi(300\ \mathrm{K}) \tag{6.2-1}$$

The calculations below are all done with the maximum values for the piezoresistive coefficients.

For the beam, case C

$$\begin{aligned} \frac{\Delta R}{R} &= \varepsilon_x(K_L + K_T) \\ &= E\varepsilon_x(\pi_L + \pi_T) \end{aligned}$$

	[10^{-11} Pa^{-1}]	
	$\pi_L + \pi_T$	$K_L + K_T$
p-type	6	10
n-type	-49	-82

It follows that n-type silicon will give a much larger sensitivity than p-type silicon, because the effective gauge factor is the sum of the longitudinal and transversal gauge factors. The effective gauge factor is 8 times larger for n-type silicon than for p-type silicon.

For case D, with the plate constriction, the solution is dependent on the geometry and resistivity of the resistor through A and B, where $A=\frac{R_{legs(2\lambda)}}{R_{total}}$ and $B=\frac{R_{top}}{R_{total}}$:

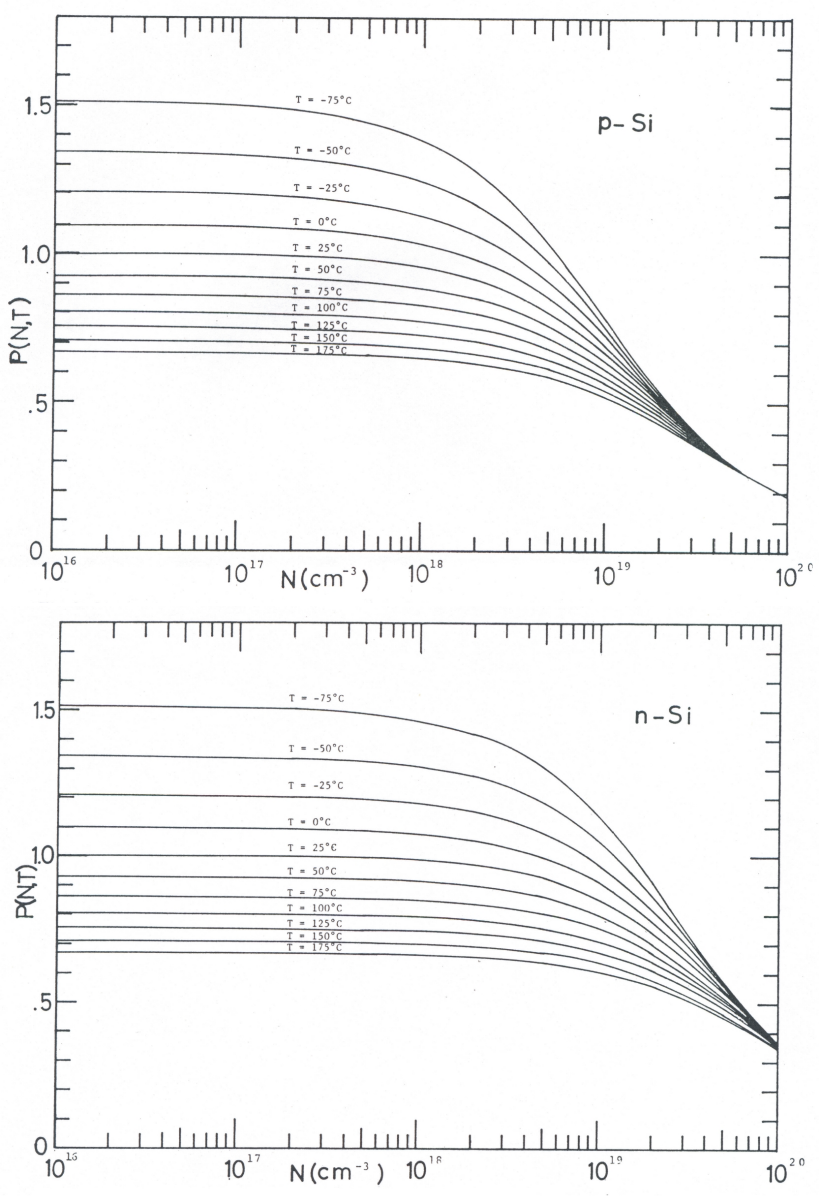


Figure 6.2: Pre-factor P used in $\pi(N,T)$=$P(N,T)\pi(300K)$ from Kanda[95]. P is plotted as a function of temperature and dopant concentration for p-type silicon (top) and for n-type silicon (bottom).

$$A = 1: \quad \frac{\Delta R}{R} = \varepsilon_x K_L$$

$$B = 1: \quad \frac{\Delta R}{R} = \varepsilon_x K_T$$

$$A = B: \quad \frac{\Delta R}{R} = \frac{1}{2}\varepsilon_x (K_L + K_T)$$

Effective gauge factor

	A=1	B=1	A=B
p-type	122	-112	5
n-type	-52	-30	-41

In the extreme cases where either A=1 or B=1, p-type will be the most sensitive solution, whereas in the case with A=B, n-type will be the most sensitive. So for a short cantilever (or resistor), the specific design of the piezoresistor will decide the preferred type of dopant. In general it can be seen that if both resistor components along and perpendicular to the length axis of the cantilever contribute, the n-type silicon will be the safe choice.

The most sensitive sensors should in principle be obtained with p-type silicon for a plate with either $A \gg B$ ($K_{\text{effective}}$=122) or $B \gg A$ ($K_{\text{effective}}$=-112). However, other design issues might come into play, as already mentioned in the above paragraph. The piezoresistors can of course be designed so that either resistors experiencing longitudinal or transversal strain dominates, and this piezoresistor can be placed near the clamping of the cantilever, but as it was seen from the FEM analysis in section 3.3, the strain component perpendicular to the length axis is not zero at the clamping, and this non-zero strain will lower the effective sensitivity of the p-type resistor.

Kassegne *et al.*[96] have previously reported on the optimisation of a cantilever sensor with single crystalline silicon optimised for measuring surface stress. They worked with finite element modelling to find the optimum placement and design of the piezoresistor. Their model, however, was limited to work for p-type silicon, and could as such not be used to say whether p- or n-type silicon gives the best sensitivity. Their result for the p-type silicon was that the resistor should be placed as close to the clamping as possible. This follows the findings from this section, since placing the resistor close to the clamping means that it is constricted like in the plate case, and the calculations above clearly showed that for p-type silicon, the sensitivity is much higher for a plate than for a beam.

The masks for the cantilever sensor are presented in the following section. The design of the cantilevers and resistors made on the SOI substrate follows the design for the cantilevers with polysilicon resistors, with a resistor that covers all of the cantilever length, and the best approximation is again to treat the cantilever as a beam since the length to width ratio is close to 4. Accordingly, the resistors will be of the n-type implanted with phosphorous.

6.3 Realisation

The sensor is made on an existing mask set[57] for convenience, since all the masks developed previously during this project have been for making cantilevers that are released from the back of the wafer in KOH. The mask set defines 2 times 5 cantilevers placed opposite each other in a channel as illustrated in the top left corner of figure 6.3. The channel is etched from the front with KOH until

the cantilevers are totally released, which with the cantilever width of 34 μm was found to be achieved with a channel depth of roughly 50 μm.

However, initial tests showed that it was very difficult to achieve an efficient resist coating near the edges of the etched channels, which again made it very difficult to define the electrical metal wiring after the KOH etch. Therefore a modified mask set was made, where the contact holes were pulled almost 300 μm away from the edge of the channel. This proved a downside of this process, which is that actual resist patterning on and close to the cantilevers with standard resist is very difficult. The definition of the metal wiring on the chip will be an etching process, and since it is a 'subtractive' process, the fact that most cantilevers are not coated with resist is not a problem.

6.3.1 Mask layout

The masks for the SOI cantilever sensor are shown in figure 6.3.

Mask (1) defines the piezoresistors and the contact pads in the silicon. The separation between the two legs of the resistors of 2 μm can not be seen on the figure.

Mask (2) is an implantation mask that allows the top of the resistor and the contact pads to be implanted with a higher concentration than the rest of the resistor. It is a reminiscence of the old masks that the top of the resistor is heavily implanted, as this part contributes to the resistance change in the same way as the legs of the resistor. On the other hand, if the series resistance of the top of the resistor is very low, it does not have a significant influence on the sensitivity.

Mask (3) defines contact holes to make contact between the contact pads and the metal wiring.

Mask (4) is for the channel and the cantilever geometry.

Mask (5) is the mask for defining the metal wiring.

Figure 6.4 depicts a close-up of the masks that define the cantilever and the resistor. The silicon contact pads on the chip have a width of 100 μm and the distance from the channel to the contact holes is 285 μm.

6.3.2 Process sequence I

The process sequence for the processing of the SOI chips is sketched in figure 6.5. SOI wafers with a buried oxide layer of 4000 Å and a top layer of 2150 Å silicon were used. A detailed process description can be found in appendix G. After

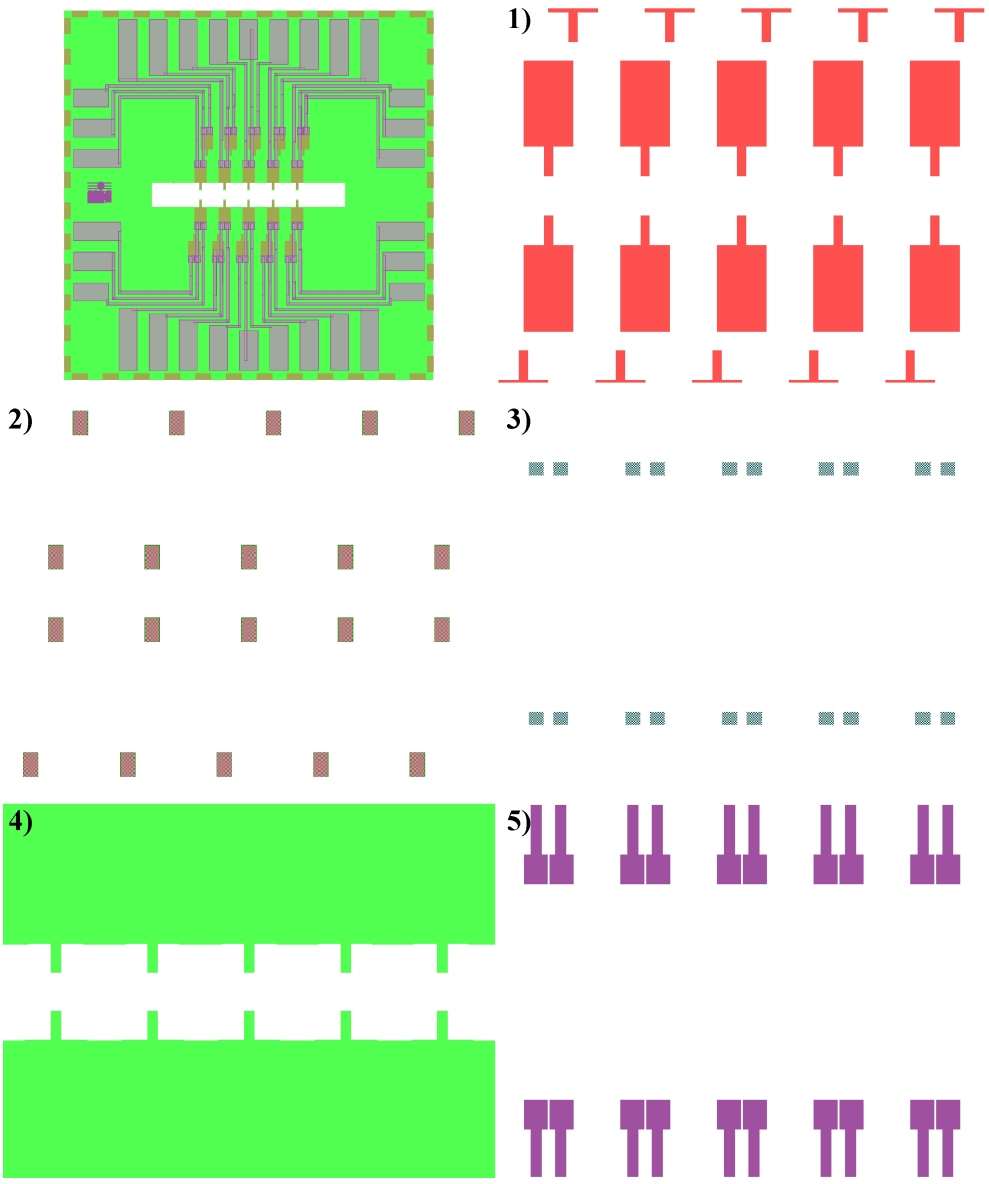


Figure 6.3: Masks for the SOI chip. The whole chip, which includes ten cantilevers in a channel, is shown in the upper left corner. The whole chip has the dimensions of 6.1×6.1 mm and the width of the channel is 400 µm. In each of the subfigures 1-5 is shown a zoom-in on the central channel part of the masks defining the sensor.

the oxide strip in diagram (g) in figure 6.5 the cantilevers bent downwards and stuck to the bottom of the channel as detailed in the SEM picture in figure 6.6. The stress levels in the silicon and silicon oxide layers on the SOI wafers are not known, but if typical values of σ_{Si}=10 MPa and σ_{SiO_2}=-300 MPa along with the measured stress of 620 MPa in the deposited silicon nitride are used, an estimate of the bending of the cantilever can be made. The radius of curvature R of a

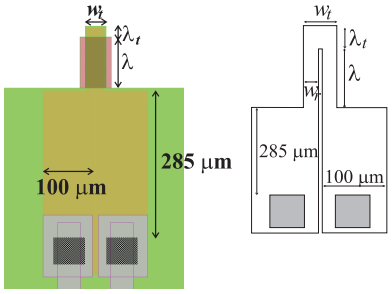


Figure 6.4: Resistor and contact pads for the SOI chip. The dimensions are w_r=16 µm, λ=106 µm, w_t=34 µm and λ_t=16 µm. To the right is a schematic drawing of the resistor(length λ), the silicon contact legs(285×100 µm^2) and contact holes(60×60 µm^2).

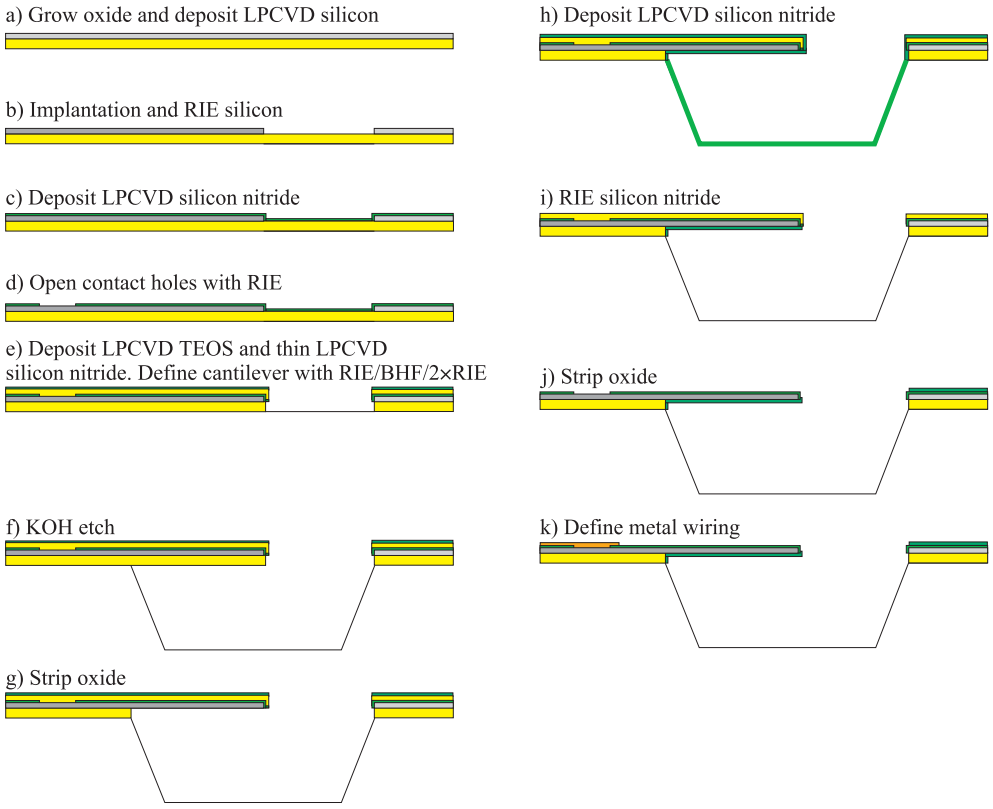


Figure 6.5: Process sequence for the SOI chip.

cantilever with in-plane stress was given as β=$1/R$ in equation 3.6-8

$$\beta = -\frac{\Sigma_i \sigma_i t_i \left(z_T - \sum_{j=0}^{i} t_j + \frac{t_i}{2} \right)}{\sum_i Y_i t_i \left((z_T - \sum_{j=0}^{i} t_j + \frac{t_i}{2})^2 + \frac{1}{3}(\frac{t_i}{2})^2 \right)} \qquad (6.3\text{-}1)$$

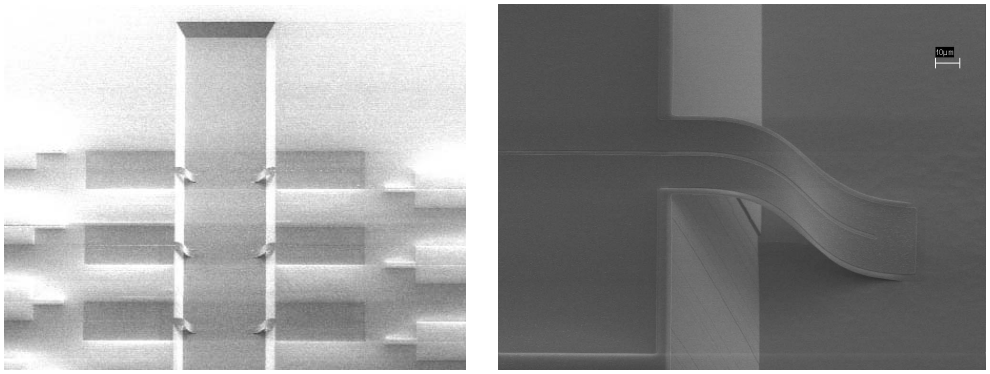


Figure 6.6: Cantilevers sticking to the bottom of the channel. The channel height and width are 50 µm and 400 µm.

The bending u of a cantilever of length L is then

$$u = \frac{1 - \cos(\beta L)}{\beta} \simeq \frac{1}{2}\beta L^2 \tag{6.3-2}$$

The bending is calculated at +37 µm before the oxide strip, figure 6.5(f), and -55 µm after the oxide strip in figure 6.5(g). This underlines the importance of controlling the bending of the cantilever during processing, and a modified process sequence was developed as a result of these findings.

6.3.3 Process sequence II

For the second batch of SOI chips, the modified process sequence is given in figure 6.7 alongside the estimated bendings u of the cantilever during processing. The main difference to the previous process is that the buried oxide is left, between step (f) and (g), before the deposition of the LPCVD silicon nitride. Only step (h) looks critical with a bending downwards of 26 µm, but since it is a dry etching process, the risk of the cantilever sticking to the bottom of the channel is minimal compared to a wet process, where capillary forces could pull the cantilever down.

Again a detailed process sequence can be found in appendix G, but the basic process steps are described below:

a Figure 6.7(a) depicts the formation of 4000 Å silicon oxide and the deposition of 2200 Å LPCVD silicon on standard wafers that are processed along with the SOI wafers as test wafers.

b The resistors are formed with RIE through the silicon and silicon oxide(mask (1)) followed by an ion implantation of phosphorus of $6.5 \cdot 10^{14}$ cm^{-2} to achieve a dopant concentration of $3 \cdot 10^{19}$ cm^{-3}. With mask (2)

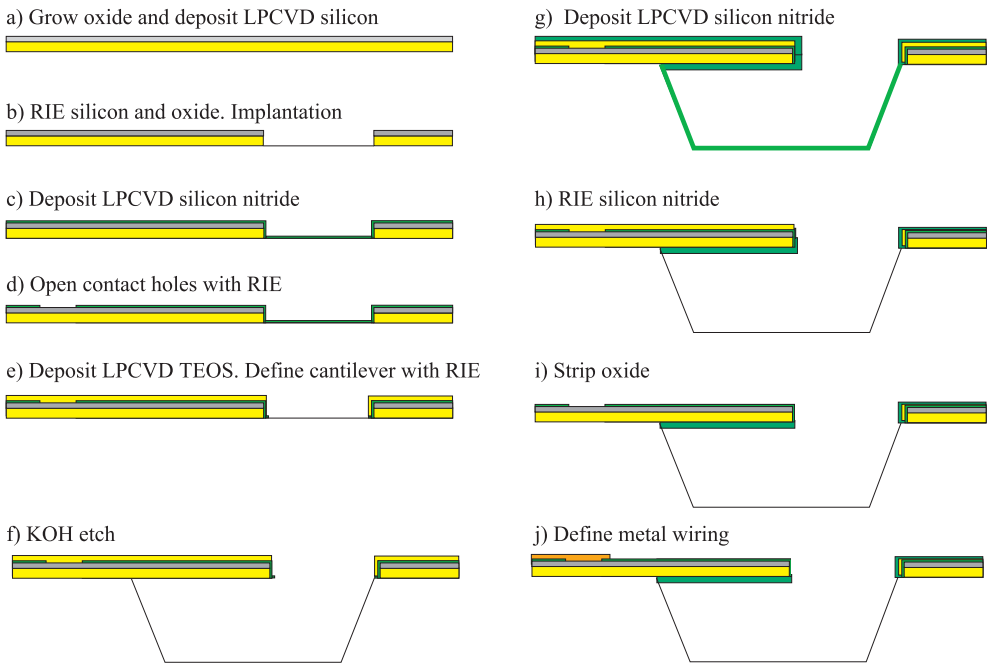


Figure 6.7: Modified process sequence for the SOI chip.
The bendings of the apex of the cantilever are estimated from equation 6.3-2 with σ_{Si}=10 MPa, σ_{SiO_2}=-300 MPa and $\sigma_{Si_3N_4}$=620 MPa:
$u_{\text{fig f}}$=37 µm, $u_{\text{fig g}}$=5 µm, $u_{\text{fig h}}$=-26 µm and $u_{\text{fig i}}$=-4 µm.

to shield the legs of the resistor, the rest of the wafer is implanted with $3.3 \cdot 10^{15}$ cm^{-2}, so the total dose in the contact pads and top of the resistor is 6 times higher than in the legs of the resistor.

c A 1000 Å thick LPCVD silicon nitride layer is deposited. This is twice as thick as in process I in order to prevent the cantilever from bending down in the channel.

d Contact holes to the contact pads are opened with RIE using mask (3).

e 4000 Å of LPCVD TEOS (silicon oxide) is deposited and the wafers are annealed to activate the dopant. This TEOS layer is a sacrificial layer that serves two purposes: it protects the contact holes to the resistors during the KOH etch in step (f) and it acts as an etch stop layer for the RIE of the silicon nitride on top of the cantilever in step (h). The cantilevers and the channel are defined with mask (4) using RIE.

f The cantilevers are released in KOH by etching the channel structure in the bulk silicon. The channel depth is 50 µm.

Silicon nitride(top)	100 nm
Silicon	215 nm
Silicon oxide	300 nm
Silicon nitride	206 nm

Table 6.3: Thickness of the thin films in the cantilever.

g A 1600 Å LPCVD silicon nitride layer is deposited. The thickness is chosen larger than the layer deposited in step (c) in order to keep the silicon resistor well above the neutral axis.

h The silicon nitride is etched selectively on top of the cantilever with an anisotropic RIE. The reason for etching the silicon nitride on top of the cantilever is to maximise the sensitivity of the sensor by moving the silicon resistor as far away from the neutral axis as possible.

i The silicon oxide is stripped in BHF.

j Titanium and gold layers are deposited and the wiring (mask (5)) is formed by etching of the metals.

During all of the process steps with released cantilevers, the cantilevers bend upwards, and no cantilevers stuck to the bottom of the channel. A mass flow controller for the silicon nitride furnace was changed shortly before the deposition of the silicon nitride in step (g) and a lower stress in this silicon nitride accounts for a smaller bending downwards than anticipated in steps (h) and (i).

The chips are separated by dicing the wafer.

The thicknesses of the thin films in the cantilever sensor are given in table 6.3. The thickness of the thin films have been measured during processing. However, the thickness of the buried oxide after the KOH (step f in figure 6.5) is only estimated from an etch rate of the silicon oxide of 20 Å/min which gives a reduction of the silicon oxide thickness of ≈100 nm.

Figure 6.8 shows SEM pictures of the finished cantilevers. The cantilevers are seen to bend 20-30 μm upwards which is not supposed to give any problems when using the cantilevers in a micro fluidic system.

6.4 Evaluation

As for the chips with polysilicon resistors, the SOI chips are characterised so an estimate of the performance of the sensor can be given.

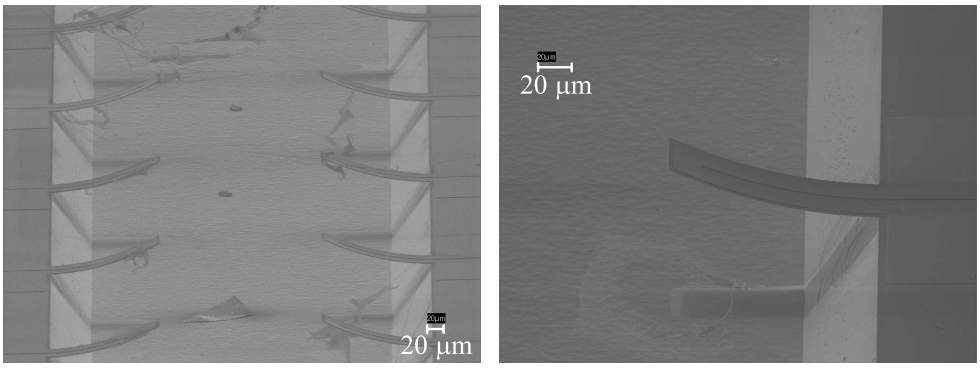


Figure 6.8: SEM pictures of cantilevers on the SOI substrate.

6.4.1 Resistivity

The total resistance of the resistor is 2.4 kΩ. The contact pads and the top of the resistor, see figure 6.4, have a higher phosphorous concentration than the legs, and if a resistivity 5 times lower than that for the legs is assumed, the resistivity ϱ of the resistor legs is found from

$$\begin{aligned} R_{total} &= R_{si\ contact\ pads} + R_{2\cdot top} + R_{2\lambda} \\ &= \frac{2\varrho}{t_{si}}\left(\frac{1}{5}\frac{285\ \mu\text{m}}{100\ \mu\text{m}} + \frac{1}{5}\frac{34\ \mu\text{m}}{16\ \mu\text{m}} + \frac{106\ \mu\text{m}}{16\ \mu\text{m}}\right) = \frac{2\varrho}{215\ \text{nm}}7.63 \\ &\Downarrow \\ \varrho &= 3.4\cdot 10^{-3}\ \Omega\cdot\text{cm} \end{aligned} \tag{6.4-1}$$

where a resistance of twice the nominal resistance of the top of the resistor is used.

6.4.2 Gauge factor

The bending sensitivity $\Delta R/R\cdot z^{-1}$ is recorded in figure 6.9. The effective gauge factor for the bending sensitivity is found from

$$\frac{\Delta R}{R} = \varepsilon_x[K_L(A-\nu B) + K_T(B-\nu A)] \tag{6.4-2}$$

given in table 3.1 for an apex force on a beam. From the numbers in equation 6.4-1 $R_{2\lambda}$=2.1 kΩ and $R_{2\cdot top}$=0.14 kΩ corresponding to A=0.94 and B=0.06. Then to a good approximation

$$\frac{\Delta R}{R} = \varepsilon_x(K_L - \nu K_T) \tag{6.4-3}$$

It can also be seen that the series resistance, $R_{si\ contact\ pads}$, is insignificant to a first approximation. The strain ε_x for the end point deflection was found in

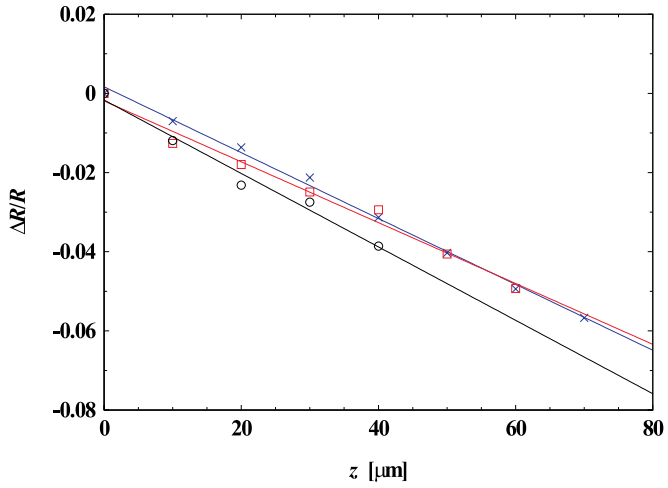


Figure 6.9: Relative resistance change as a function of the bending of the cantilever. Tests of cantilevers on three different chips are plotted. The three different slopes of $-9.27 \cdot 10^{-7}$ nm^{-1}, $-7.69 \cdot 10^{-7}$ nm^{-1} and $-8.32 \cdot 10^{-7}$ nm^{-1} corresponds to effective gauge factors of -43, -36 and -39 with an average of -39.

section 3.5 on page 27. The effective gauge factor from figure 6.9 of -39 then equals $K_L - \nu K_T$. If the same relation between the longitudinal and transversal gauge factor as listed in table 6.2 is used, then K_L/K_T=52/30=1.7 and with a Poisson's ratio of 0.25

$$K_L = -46 \text{ and } K_T = -26$$

In figure 6.10, which is the same as figure 6.2 for n-type silicon, it can be seen that the pre-factor $P(3 \cdot 10^{19}\ \text{cm}^{-3}, 25°\text{C})$ is approximately 0.7. Thus expected gauge factors would be approximately K_L=-36 and K_T=-21 when following the theory of Kanda. The large difference between expected and measured values can be due to the uncertainties connected with the measurement of the bending sensitivity and the calculation of the gauge factor. For the measurement the largest uncertainty is from the placement of the needle that presses the cantilever down, and from the calculations an error will be on the thicknesses of thin films, *e.g.* the silicon oxide under the silicon resistor. The bending sensitivity is given as

$$\frac{\Delta R}{R} z^{-1} = \frac{k(L - \frac{\lambda}{2})d}{EI} K_{effective} = \frac{3(L - \frac{\lambda}{2})d}{L^3} K_{effective} \qquad (6.4\text{-}4)$$

If, as an example, the needle makes contact with the cantilever at a distance Δx away from the apex, then the effective length is L_e=$L - \Delta x$. If Δx=10 μm for the given dimensions with L=130 μm and λ=106 μm, then the effective strain in the piezoresistor would be

$$\left(\frac{L_e - \frac{\lambda}{2}}{L_e}\right) / \left(\frac{L - \frac{\lambda}{2}}{L}\right) = 1.1$$

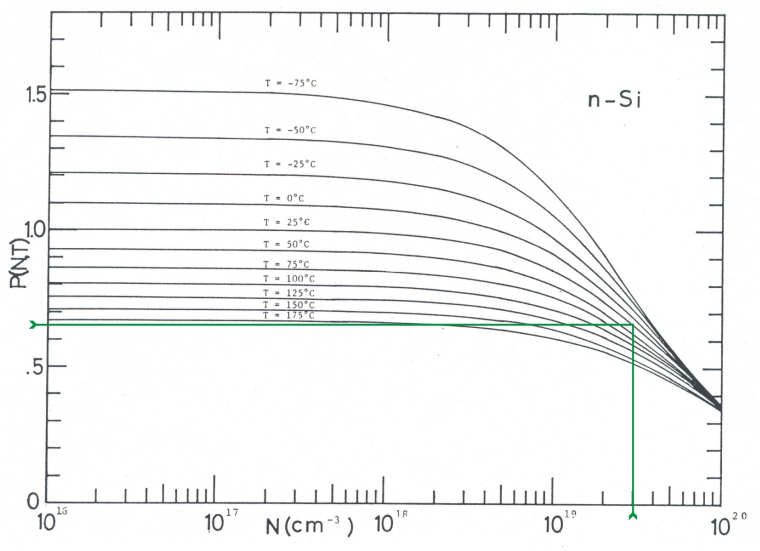


Figure 6.10: Pre-factor $P(N,T)$ as a function of temperature and dopant concentration for n-type silicon[95]. The added line shows $P(N,T)\simeq 0.7$ for 25°C and $N=3\cdot 10^{19}$ cm^{-3}.

times higher than the apparent measured strain, and hence the gauge factor would be overestimated by the same amount. For Δx=20 µm the error is 1.2. The error of the thickness goes with the first power through d, which is the distance from the neutral axis to the piezoresistor, but here the error on the gauge factor can go both ways.

What is needed in future mask sets are test structures that makes a determination of the longitudinal as well as the transversal gauge factor possible.

6.4.3 Expected performance

The expected performance is calculated with the gauge factors K_L=-46 and K_T=-26 found above. With these values the effective gauge factor for a surface stress measurement on a cantilever beam is -72, since the sensitivity is given by

$$\frac{\Delta R}{R}\sigma_s^{-1} = \varepsilon_x(K_L + K_T)\sigma_s^{-1} \tag{6.4-5}$$

The estimated sensitivity and resolution $\sigma_{s\ min}$ are given in table 6.4. Compared to the best data obtained for polysilicon, see table 5.5 on page 65, the sensitivity is twice as high and the resolution is more than six times better.

k [N/m]	f [kHz]	$\sigma_{s\ min}$ [N/m]	$\frac{\Delta R}{R}\sigma_s^{-1}$ [(N/m)$^{-1}$]
0.54	71	$1.4 \cdot 10^{-4}$	$9.6 \cdot 10^{-4}$

Table 6.4: The calculated performance of the cantilever stress sensor with the thin film thicknesses $t_{ni\ top}$=100 nm, t_{si}=215 nm, $t_{si\ ox}$=300 nm and $t_{ni\ bottom}$=206 nm, and with ϱ=3.4 $\cdot 10^{-3}$ Ω·cm, K=-72, V_{in}=5 V and Δf=1-51 Hz. An alpha value of α=6 $\cdot 10^{-6}$ is used as an estimate for the single crystalline silicon[25, 68].

Optimised SOI and comparison to optical readout

This is obtained with a mask design that is not optimised for single crystalline silicon resistors. By optimising for the resolution $\sigma_{s\ min}$ with the same parameters as above, it is possible to give an estimate of the best obtainable resolution for the SOI sensor. The obtained values are

$$\begin{aligned} \sigma_{s\ min} &= 3.8 \cdot 10^{-5}\ \text{N/m} \\ \frac{\Delta R}{R}\sigma_s^{-1} &= 2.0 \cdot 10^{-3}\ (\text{N/m})^{-1} \end{aligned} \tag{6.4-6}$$

for the optimised dimensions

$$\lambda$=418 μm, t_{si}=101 nm, t_{ox}=80 nm, $t_{ni\ bottom}$=105 nm

see figure 6.11, and the other geometrical factors locked: w_r:=50 μm, λ_t:=20 μm and $t_{ni\ top}$:=50 nm. This means that it should be possible to improve the sensi-

Figure 6.11: Schematic outline of cross section of the optimised SOI cantilever.

tivity with a factor of two and the resolution with more than a factor of three compared to the present SOI design. With λ=418 μm the spring constant is only 0.002 N/m, but if λ is reduced to 200 μm the spring constant goes up to 0.02 N/m and the resolution only drops to $4.4 \cdot 10^{-5}$ N/m.

Under the discussion of thermal vibrational noise in chapter 3, the noise on surface stress was estimated by

$$\sigma_{sv_{\Delta f}} = k_{\sigma_s} z_v = \frac{2EI}{wdL^2} z_v \tag{6.4-7}$$

where $z_v \approx \sqrt{\frac{2k_B T \Delta\omega}{\pi k Q \omega_{res}}}$. This value can be considered the lowest measurable surface stress in a system without electrical noise in the piezoresistors. With a quality factor of 1 and a resistor length of λ=200 μm and the dimensions and bandwidth

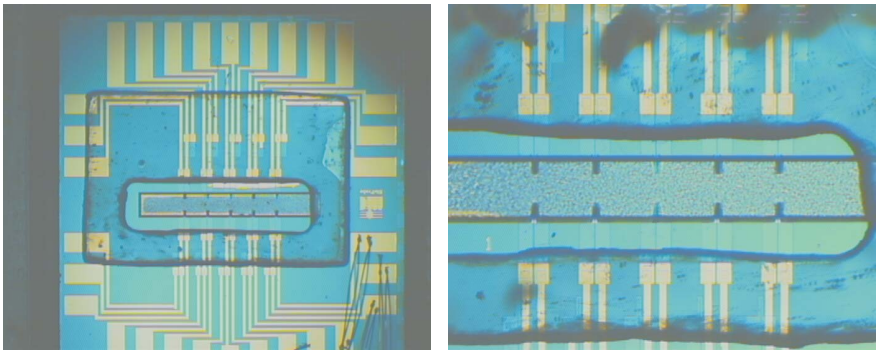


Figure 6.12: PDMS on the chip. The pictures show two different chips. The crucial thing is to place the PDMS so that it covers the gold wiring. On the chip to the left wire bonding on the gold contact pads can be seen.

used above, $\sigma_{sv_{\Delta f}}$=1.4 · 10^{-5} N/m (z_v = 0.3 Å) or only three times lower than the resolution for the optimised SOI sensor, meaning that thermal vibrational noise has to be taken into account and, meaning that the resolution of a cantilever with single crystalline silicon in principle can come close to the limit given by the thermal vibrational noise.

6.4.4 Test in biochemical setup

The chips were tested in a liquid environment primarily to check the quality of the silicon nitride encapsulation. A first test was to fill the channel and cover the cantilevers in a buffer containing 0.1 M NaCl to see whether the signal would be stable, which would indicate that the piezoresistors are fully encapsulated in the silicon nitride. To do that the silicon chip needed a packaging that could prevent the buffer from reaching the gold wiring[97]. The first packaging step is shown in figure 6.12. A PDMS layer is placed on the chip and is shaped, so that it will act as the top of the walls in the liquid channel. A lid of PMMA is glued on top to close the channel. In this experiment the liquid is not flowing, but small pipes for liquid inlet and outlet can be placed in the PMMA lid if necessary.

A chip was tested by running a temperature cycle changing the temperature between 30°C and 40°C, and a section of the output signal from the Wheatstone bridge is plotted in figure 6.13. What is seen is a voltage signal from the Wheatstone bridge caused by the fact that the bridge is never balanced perfectly. In the figure to the right the off-set voltage measured in air is plotted. A noise level of only a few μV can be seen, which looks very promising. However, during the tests in liquid the off-set voltage of the Wheatstone bridge made some abrupt changes from only a few μV to a few mV, which could indicate a possible short circuit that appeared and disappeared again, though an explanation for the physics be-

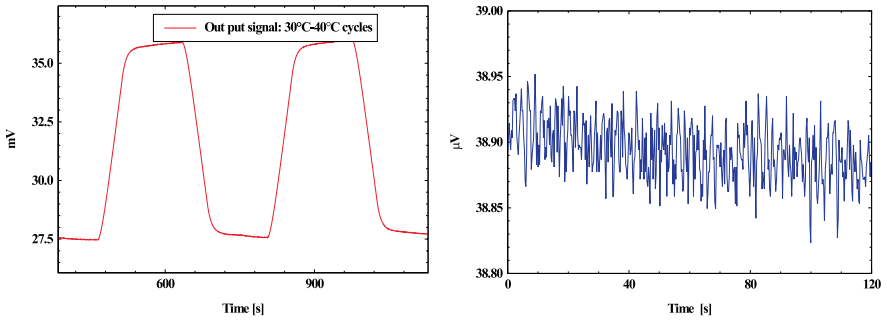


Figure 6.13: Left: Output voltage from Wheatstone bridge. The temperature is cycled between 30°C and 40°C for 3600 s. The chip is kept at a constant temperature at 30 and 40°C for 120 s. Right: Off-set voltage in air showing p-p voltage of less than 2 µV.

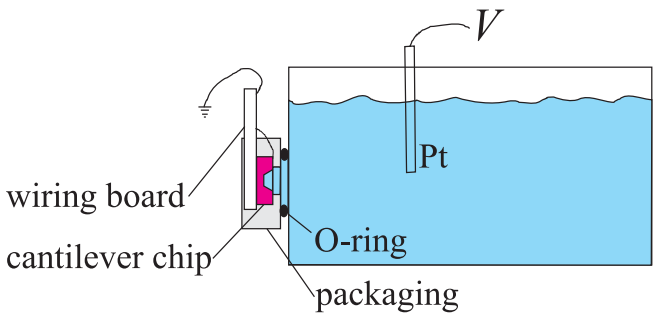


Figure 6.14: Electrolytic cell where the chip is tested for leak currents.

hind is difficult. This behavior indicates that there could be a problem with the encapsulation of the piezoresistors.

To check this, another chip was tested for leak current in an electrolytic cell as sketched in figure 6.14. The cell is filled with a buffer solution containing salts. The cantilevers are exposed to the buffer through a hole in the container. The chip is pressed against an O-ring to keep the connection tight. When applying a voltage of 1.5 V to the platinum electrode in the buffer, a current of 0.13 µV was running between the electrode on the chip and the platinum electrode. This shows that there is a possibility for a leak current to pass from the solution to the circuit on the chip, *i.e.* the piezoresistors are not properly encapsulated or there is a leak underneath the PDMS layer that seals the gold wiring from the liquid.

Since both tests gave problems with different chips, and the packaging scheme is often used on other chips with good results, the most plausible explanation

is that the coating on the chips is not good enough. When inspecting the chips

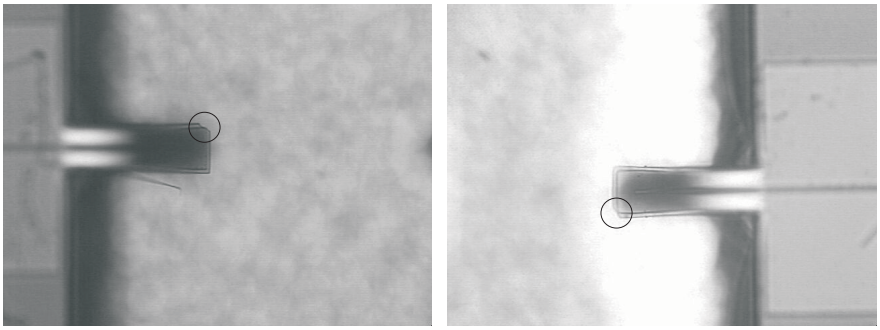


Figure 6.15: Optical pictures of cantilevers. On both cantilevers the silicon nitride is damaged on a corner at the apex. Due to the bending only the apex is in focus.

under microscope it is seen that many of the cantilevers have sustained damages somewhere during processing, see examples in figure 6.15. For the liquid test only chips that passed the optical inspection were used, but the tests indicate that damages to the silicon nitride coating that are not visible under microscope are present. As the visible damages appear at the edge of the cantilevers it is reasonable to guess that the silicon nitride is etched in the RIE process - see process sequence in figure 6.7, diagram (h) - that should only remove the silicon nitride on top of the cantilever. The TEOS oxide mask and the underlying silicon nitride, which it should protect, is formed with the same mask (diagram (e)), so the TEOS oxide is only covering the top of the silicon nitride. If a larger mask was to be used for the TEOS oxide, then the edges of the cantilever would be better protected, and a better encapsulation of the piezoresistors would be expected.

6.5 Summary

A first generation surface stress sensor on an SOI platform was presented and realised. The sensor features a piezoresistor encapsulated in LPCVD silicon nitride. However, the resistor was not totally encapsulated in silicon nitride which is attributed to an RIE process that can attack the silicon nitride. This is a problem that should be solvable with a new mask set that is specifically made for the SOI sensor, instead of the mask set used here that was developed for another cantilever sensor.

For the design of the SOI sensor it was found that n-type silicon makes the most sensitive sensor when measuring uniform in-plane surface stress. This applies to a cantilever beam where the longitudinal and the transversal strain by nature is the same. This is opposite the design for AFM cantilevers, where the

largest strain is along the length of the cantilever, and the high gauge factor of p-type silicon along [110] on a (100) surface makes the best choice. For the surface stress sensor with piezoresistors near the clamping of the cantilever, the optimal choice of dopant becomes dependant on the geometry of the resistor, and in order to fully understand the behavior of the strain in this region, a FEM analysis is recommended.

The longitudinal gauge factor of the single crystalline silicon was determined at -46. Test structures for individual measurements of the longitudinal and the transversal gauge factor could improve the determination of the effective gauge factor and hence the quality of the estimate of the sensitivity.

It was shown that the theoretical resolution limit for the SOI sensor is comparable to the resolution limit set by thermal vibrational noise.

Chapter 7

Cantilever chip in SU-8

As a new technology platform that could supplement or replace the silicon platform from the previous chapters, we have worked on a chip made entirely from the photoresist SU-8[98] since 2002. The chips described in this chapter have been developed together with Montserrat Calleja, who is a post doc in the Bioprobe group at MIC.

Along the same lines as for the silicon based sensors, the SU-8 based sensor is being encapsulated so that it can be applied in wet biochemical measurements. The objective is to develop a liquid handling chip with an incorporated array of cantilevers made entirely from SU-8, where silicon wafers are only used as carrier substrates during processing. By making the cantilevers and the channel structure in the same process and from a polymer, the processing is potentially cheaper than the fabrication of conventional silicon chips that are subsequently integrated with for example a polymer packaging.

SU-8 is already being extensively used for making micromachined liquid channels[99, 100].

7.1 Cantilevers in SU-8

Genolet *et al.*[101, 102] were the first to report on cantilevers made from SU-8 in 1999. They made cantilevers for use in AFM with optical readout.

Thaysen *et al.*[103] presented in 2002 an SU-8 cantilever with readout from integrated strain gauges made of gold. They argue that an SU-8 cantilever with metal strain gauge will have a sensitivity comparable to that of a silicon cantilever with a piezoresistive silicon strain gauge. This comes about since the sensitivity $\Delta R/R$ is proportional to the gauge factor over the Young's modulus K/E, see *e.g.* the results in table 3.1 on page 22. With a gauge factor for the metal of 2

and a Young's modulus of 5 GPa for the SU-8 then $K/E_{\mathrm{SU-8}}$=0.5 GPa^{-1}. For silicon with gauge factors in the range of 30-100 and a Young's modulus of 170 GPa K/E_{silicon} is 0.2-0.6 GPa^{-1}.

7.2 Design

Basically two design approaches have been investigated, and they are sketched in figure 7.1.

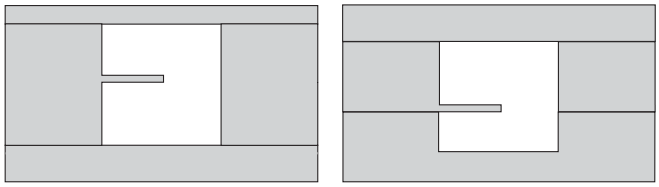


Figure 7.1: Cross section of channel with integrated cantilever. To the left: Cantilever and channel structure made in one process sequence. To the right: Cantilever and top part made in one chip and glued to another chip defining the bottom part of the channel.

One approach is to fabricate a true free hanging cantilever in one SU-8 chip, and then just glue a lid on the structure to complete the micro liquid channel.

The other approach is to make two SU-8 chips, one including a cantilever and one half of the liquid channel and a second including the other half of the channel. Another unstructured lid is still needed to close the top of the channel as shown to the right in figure 7.1.

For the second approach the assembly is a bit more difficult than for the first approach, because of the aligning of the two parts of the channel. However, this process is technologically more straight forward, since the cantilever structure is made as the first layer on the support wafer as shown in figure 7.2 (right). In the

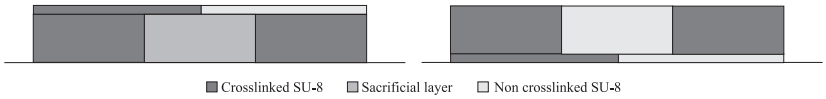


Figure 7.2: The 1st and the 2nd approach.
1st: Sacrificial layer in channel to support the SU-8 for the cantilever layer on top.
2nd: Widest SU-8 structure made first so that exposure of underlying SU-8 layers is not a problem.

first approach the free hanging cantilever needs some kind of sacrificial layer in

the channel to act as a support for the SU-8 layer for the cantilever as shown in figure 7.2 (left).

7.2.1 The 1st approach

The first approach was investigated, but it was found that it was a very difficult task to make the free hanging cantilevers in SU-8. In the literature especially buried channels in SU-8 have been described. The technique for realising this should in principle be applicable for making free hanging cantilevers. As a requirement to the process when producing cantilevers, the technique should be able to make reasonably thin layers in order to achieve sensitive cantilevers since the sensitivity is inversely proportional to the thickness. The limit was chosen at a maximum of 10 μm, since with the 2nd approach a total cantilever thickness for the SU-8/Au/SU-8 layers of less than 5 μm is achievable.

Guérin *et al.*[104] have reported on making buried channels in SU-8 using two techniques:

a) Using an underfill/sacrificial layer in the channel to planarise and then spin and crosslink SU-8 on top.

b) Leaving the non-exposed and non-crosslinked SU-8 in the channel and use this as a planarising layer as shown in figure 7.3. Subsequently a metal layer is deposited on top to act as a UV shield to prevent the underlying SU-8 from being crosslinked, when the cantilever is structured on top. In the last process step the metal is etched and the non-crosslinked SU-8 is removed with the standard developer. With these techniques they produce channels with heights down to 50 μm, and in principle the top layer thickness is only limited by the spinning of the resist.

Tseng *et al.*[105] report on UV dosage control to make buried channels. By this technique they achieve top layer thicknesses down to 14 μm.

Tay *et al.*[106] have produced both buried channels and cantilevers using a proton beam. They make a channel with a height of 25 μm and a top layer thickness of approximately 10 μm.

Kudryashov *et al.*[107] have recently used e-beam lithography to produce free hanging structures with dimensions of a few microns.

All these techniques have been considered for making the cantilevers. However, e-beam and proton beam equipment is not available at MIC, but especially the e-beam technique seems very powerful and looks like an obvious candidate, though it can be argued that this process is neither cheap nor fast.

The UV dosage control has been tested but it is not capable of producing anything close to the required limit of less than 10 μm[108].

The solution from Guérin *et al.* with the non-crosslinked SU-8 providing the planarisation in the channel structure seemed the most straight forward and promising one, having the available equipment in mind, and the first tests with this technique were actually initiated before this article was found.

The process has been tested with different thicknesses of SU-8, from a few microns to more than 100 microns, and with different kinds of metals as UV shields, see figure 7.3. The UV shield in principle works since it prevents crosslinking of

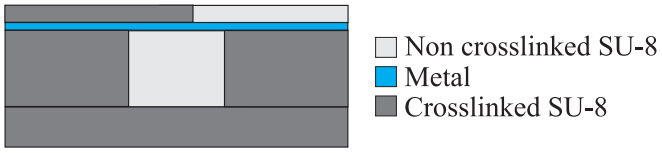


Figure 7.3: Metal UV shield for preventing underlying SU-8 from being exposed during processing of cantilever structure on top.

the SU-8 underneath during subsequent UV exposures. However, it is found that the deposition of the metal by e-beam evaporation alone makes the top of the unexposed SU-8 crosslink, making it impossible to obtain thin cantilever structures. A thorough description of the considered and tested approaches can be found in the master's thesis of Johansson[108].

7.2.2 The 2nd approach

The chips realised so far have been made using the 2nd approach, where the top and the bottom part of the channel have been fabricated separately and glued together.

7.2.3 Mask set

The masks are drawn in figure 7.4. The first five masks are for defining the top part that includes the cantilever with integrated strain gauge.

Mask (1) defines the bottom of the cantilever.

The second mask is for the metal wiring on the chip.

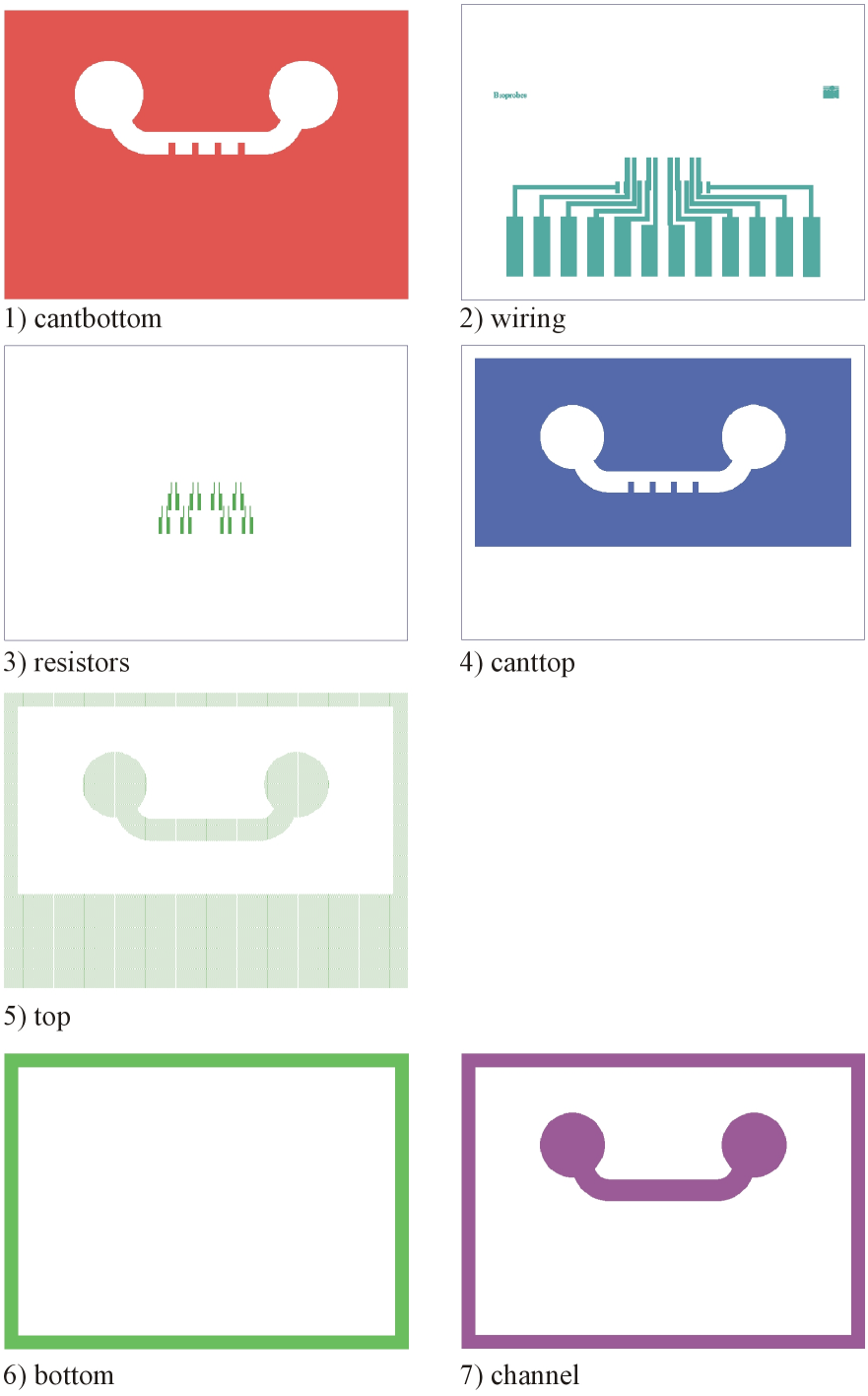


Figure 7.4: The mask set for the SU-8 chip. Mask 1-5 are for the top part including the cantilever and mask 6-7 are for the bottom part of the liquid channel.

Mask (3) is defining the metal resistor structure on the cantilevers. The re-

sistor is formed like a meander structure.

Mask (4) is for encapsulating the top of the cantilever in the SU-8.

Mask (5) is defining the top of the walls in the liquid channel.

Mask (6) is defining the bottom of the liquid channels and mask (7) is for the bottom part of the channel walls.

7.3 Realisation

The process sequence for the SU-8 chip is given in figure 7.5. Figures (a)-(e)

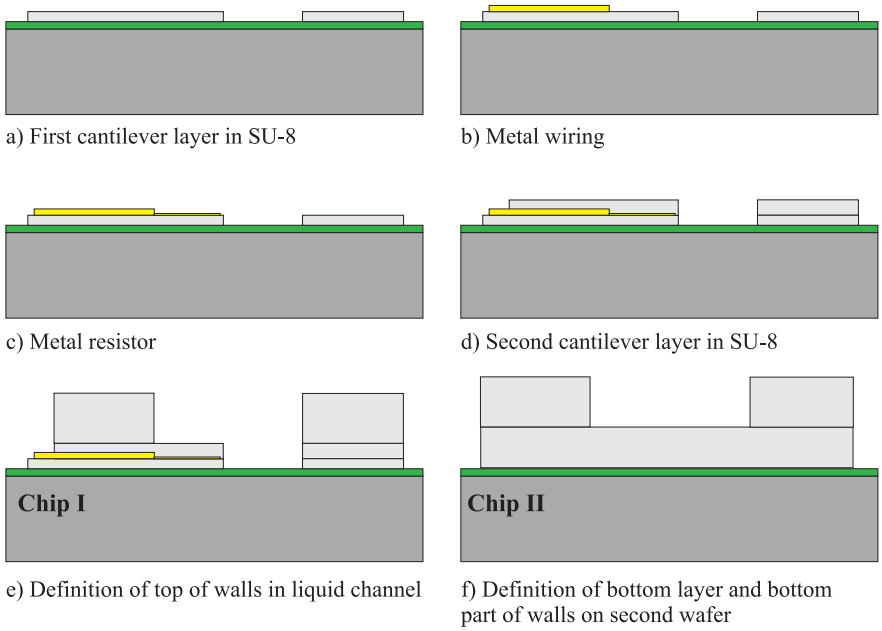


Figure 7.5: Process sequence for the SU-8 chips. Figures (a)-(e) describe the processing of the cantilever part and figure (f) describes the other part of the channel.

describe the processing of the cantilever part and figure (f) describes the other part of the channel.

a Chromium/gold/chromium layers with the thicknesses 5 nm/50 nm/50 nm are deposited on a silicon wafer. The top chromium layer is a fast etching sacrificial layer that is etched when releasing the SU-8 chip from the substrate[109]. The first SU-8 layer for the cantilever is patterned. The thickness is 1.7 µm.

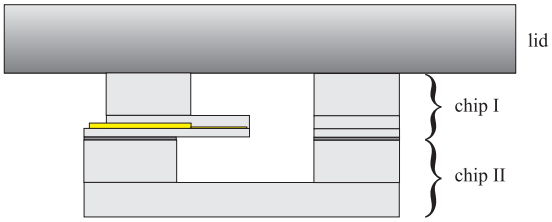


Figure 7.6: Assembly of the two SU-8 chips. The top of the channel is sealed with a PMMA lid.

b Titanium/gold wiring is defined with wet etching. The thicknesses are 2 nm and 800 nm.

c Titanium/gold resistors are defined with wet etching. The thicknesses are 2 nm and 40 nm.

d The second SU-8 layer for the cantilever is patterned. The thickness is 4.5 µm.

e The walls of the liquid channel is defined in a 100 µm layer of SU-8.

f The bottom and the walls for the other part of the channel is made on another silicon substrate. A release layer of chromium/gold/chromium is used again.

After release etching of the cantilever chip, in figure 7.5 (e), it is glued together with the bottom part. This is done by spinning a thin layer of SU-8 on the wafer holding the structure in figure 7.5 (f). While keeping the wafer on a hotplate at 75°C, the cantilever part is manually brought in contact with the bottom channel part. This is done under a microscope for aligning. Afterwards the SU-8 at the joint parts of the SU-8 structures are exposed with UV light in a mask aligner followed by post baking to crosslink the resist. The channel is rinsed with the developer for the SU-8. Finally a PMMA lid is glued to the SU-8 chip with a layer of PDMS. The assembling of the chip is shown in figure 7.6. Optical images of the assembled chips are shown in figure 7.7.

7.4 Evaluation

So far only few working chips have been realised. Some of the problems are:

- Definition of the gold resistors as they are defined by spinning normal resist over a structured surface, see figure (c) in 7.5.

- Sometimes low adhesion between the first and the second SU-8 layer in the

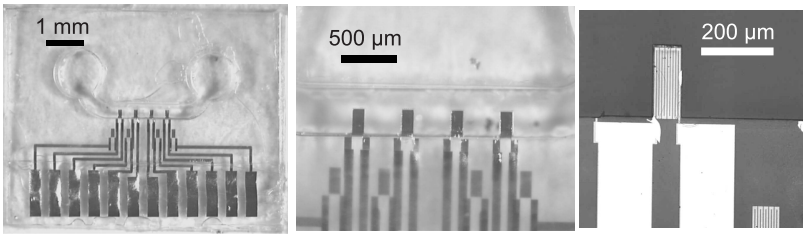


Figure 7.7: Optical images of the assembled chips before putting on the PMMA lid[110].

cantilevers. This is probably due to the processing of the metal layers on the first SU-8 layer, which leaves it with a totally crosslinked and inert surface.

But the main problem has been to make stable electrical contacts to the gold wiring on the SU-8 chip, as standard wire bonding is not applicable. This is most likely because of a combination of the ultrasonic welding on the relatively soft SU-8 substrate and a poor adhesion of the wiring to the SU-8. Wire bonding tests performed at DELTA Micosystems[111] showed that the bonding between bond wire and metal wiring on the chip could be made, but a pull load of only 0.3 grams could pull the wiring and bond pad off the chip, see test sequence in figure 7.8. Some working devices have been made with the use of a conducting glue

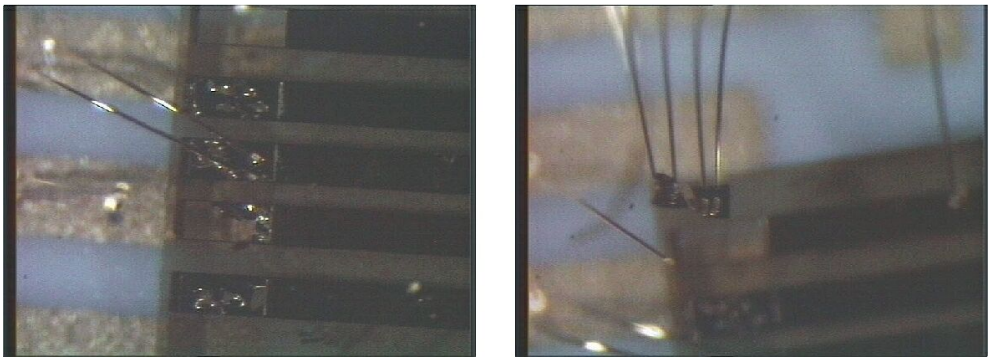


Figure 7.8: Wire bonding on an SU-8 chip. The wire bonding to the chip is shown in the figure to the left. To the right the metal wiring and bond pad is lifted off probably due to the ultrasonic welding and bad adhesion of the metal wire[111].

containing silver particles, but a more reproducible and faster way of contacting the chips is being pursued. The suggested solutions are *e.g.* anisotropically conducting glue and flip chip bonding[108].

7.4.1 Gauge factor

Bending sensitivity tests have been performed on some of the working devices. One such test is shown in figure 7.9. The sensitivity is comparable to that of the

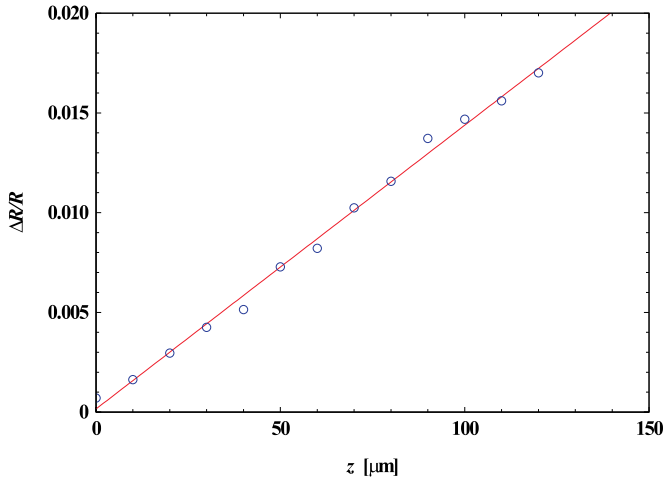


Figure 7.9: Relative resistance change as a function of bending. The slope $\frac{\Delta R}{R} z^{-1}$ is $1.4{\cdot}10^{-7}$ nm^{-1} corresponding to a gauge factor of 3.

polysilicon resistors and corresponds approximately to a gauge factor of 3.

7.5 Performance

A gauge factor of 3 is found in the case of a force applied at the apex of the cantilever. The relative resistance change of the metal strain gauge consists of a pure geometrical contribution $\Delta R/R_{\text{geometrical}}$ and a contribution from other sources $\Delta R/R_{\text{piezo}}$:

$$\frac{\Delta R}{R} = \frac{\Delta R}{R}_{\text{geometrical}} + \frac{\Delta \rho}{\rho}_{\text{piezo}} \tag{7.5-1}$$

and similarly for the gauge factor

$$K = \frac{\Delta R}{R}\frac{1}{\varepsilon} = K_{\text{geometrical}} + K_{\text{piezo}} \tag{7.5-2}$$

where ρ is the resistivity. The piezo-term originates from a change in conductivity in the strained metal crystal, from electron transfer between the grains in polycrystalline metal films and from the change in the thickness of the metal film when the thickness is comparable to the mean free path length of the electrons[112]. The first effect determines the bulk properties of the film, the second is very dependent on deposition conditions and thickness of the film, and the last is a function of the film thickness for thin films. For thin films the surface roughness

of the metal film will give a further contribution to the resistivity change[113]. According to Parker *et al.*[112] the bulk condition apply to thicknesses from about 1000 Å and up, since the mean free path length l for electrons in metals typically lies in the range of 2-800 Å. For gold $l \simeq 350$ Å[113, 114]. At the other end of the spectrum with thin films in the range of ∼100 Å and down, discontinuous films with very high gauge factors (20-100) can be obtained[112, 115, 116]. In these very thin films the conduction is dominated by tunnelling currents between the the grains or metal 'islands'. In an intermediate range with thicknesses around the mean free path length of the electrons, the scattering of electrons on the boundaries of the metal film dominates.

For a strain gauge as outlined in figure 7.10, with a current running along its length and with x being the length axis of the cantilever and y and z running along the width and height of the resistor, respectively, the pure geometrical relative resistance change can be written as a function of the strains ε_x, ε_y and ε_z. For the silicon piezoresistors dealt with so far the geometric effects on the

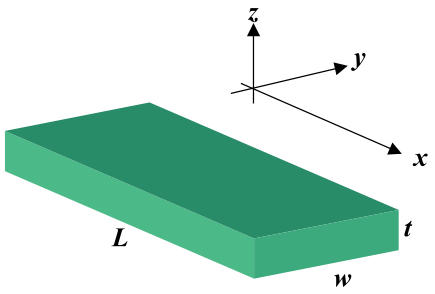


Figure 7.10: Strain gauge with current running along the length of the resistor.

resistance change as a function of strain was considered negligible since the resistance change was dominated by the piezoresistive effect. The relative geometrical resistance change for the strain gauge is given by

$$\left.\frac{\Delta R}{R}\right|_{\text{geometrical}} = \frac{(1+\varepsilon_x)}{(1+\varepsilon_y)(1+\varepsilon_z)} - 1 \qquad (7.5\text{-}3)$$

For the apex force applied at the end of the cantilever for testing the bending sensitivity, the strains in a cantilever beam, which allows free Poisson contraction in both y and z, are:

$$\varepsilon_y = \varepsilon_z = -\nu\varepsilon_x$$
$$\varepsilon_x = \sigma_x / E$$

with ε_x given as a function of the bending in equation 3.5-4. From this the relative resistance change is

$$\begin{aligned}\frac{\Delta R}{R}_{\text{geometrical}} &= \frac{(1+\varepsilon_x)-(1+\varepsilon_y)^2}{(1+\varepsilon_y)^2} \\ &= \frac{\varepsilon_x(1+2\nu)-\nu^2\varepsilon_x^2}{1+\nu^2\varepsilon_x^2-2\nu\varepsilon_x} \cong (1+2\nu)\varepsilon_x \end{aligned} \quad (7.5\text{-}4)$$

For the thin gold strain gauges totally encapsulated in SU-8 considered here, the strain of the SU-8 can be assumed to determine the strain in the gold, so that the Poisson's ratio is that of the SU-8. Normally a gauge factor of 0.22 is used for SU-8 (reported by SOTEC Microsystems, a supplier of SU-8).

The gauge factor from the piezoresistive effect K_{piezo} is given by[112]:

$$\begin{aligned} K_{\text{piezo bulk}} &= 1+2G(1-2\nu) \quad \text{for the thick film} \\ K_{\text{piezo int}} &= \nu \quad \text{for the intermediate range} \end{aligned} \quad (7.5\text{-}5)$$

where G is Grüneisen's constant which is 3.0 for gold[113]. With a Poisson's ratio of gold of 0.42 the sum of the geometrical and piezoresistive effects gives K_{bulk}=3.8 for the thick film and K_{int}=2.3 for the intermediate film. If instead the Poisson's ratio of SU-8 is used the values are 5.8 and 1.7, and hence the gauge factor of 3.0 found above lies in the range expected from theory.

7.5.1 Surface stress on cantilever

The general assumption of a geometrical gauge factor of 1+2ν for metal strain gauges lies behind the present design of the SU-8 cantilevers. In this section the theoretical sensitivity for a metal strain gauge in a cantilever is calculated for the case of a uniform isotropic in-plane (xy) stress, exactly as it was done for the cantilevers with silicon strain gauges.

If the metal film is assumed to lie in the intermediate range, where the electron transport is dominated by scattering from the film surfaces, an estimate for the piezoresistive term can be given that depends on the strain in the film. The pure piezoresistive gauge factor of ν found in the above case originates from the assumption that the resistivity ρ depends on the film thickness t according to ρ=constant/t [112]. Then

$$\frac{\mathrm{d}\rho}{\rho} = -\frac{\mathrm{d}t}{t} = -\varepsilon_z \quad (7.5\text{-}6)$$

and ε_z=$-\nu\varepsilon_x$ so that

$$K_{\text{piezo int}} = \frac{\mathrm{d}\rho}{\rho}\frac{1}{\varepsilon_x} = \nu \quad (7.5\text{-}7)$$

For the cases with in-plane stress it will in the following be assumed that the piezoresistive contribution is described by equation 7.5-6.

Again the strain will be found for two cases:

A: beam conditions

B: near clamping.

For the beam conditions σ_x=σ_y and ε_x=ε_y:

$$\begin{aligned} \varepsilon_x &= \varepsilon_y = \frac{\sigma_x(1-\nu)}{E} \\ \varepsilon_z &= -\frac{2\nu\sigma_x}{E} = -\frac{2\nu\varepsilon_x}{1-\nu} \end{aligned} \tag{7.5-8}$$

and following from equation 7.5-3

$$\frac{\Delta R}{R}_{\text{geometrical}} = \frac{2\nu\varepsilon_x}{1-\nu-2\nu\varepsilon_x} \cong \frac{2\nu}{1-\nu}\varepsilon_x \tag{7.5-9}$$

yielding a total gauge factor of

$$K_A = \frac{\Delta R}{R}_{\text{geometrical}}\frac{1}{\varepsilon_x} + \frac{\mathrm{d}\rho}{\rho}\frac{1}{\varepsilon_x} = \frac{4\nu}{1-\nu} \tag{7.5-10}$$

The gauge factor K_A is 1.1 with a Poisson's ratio of 0.22.

Near the clamping the transversal strain ε_y along the width of the cantilever is assumed to be zero, while free contraction is still assumed in the z-direction:

$$\begin{aligned} \varepsilon_x &= \frac{\sigma_x(1-\nu^2)}{E} \\ \varepsilon_z &= -\frac{\nu\varepsilon_x}{1-\nu} \end{aligned} \tag{7.5-11}$$

The gauge factor K_B is then found from

$$\frac{\Delta R}{R}_{\text{geometrical}} = \frac{\varepsilon_x}{1-\nu-\nu\varepsilon_x} \cong \frac{1}{1-\nu}\varepsilon_x \tag{7.5-12}$$

and

$$K_B = \frac{\Delta R}{R}_{\text{geometrical}}\frac{1}{\varepsilon_x} + \frac{\mathrm{d}\rho}{\rho}\frac{1}{\varepsilon_x} = \frac{1+\nu}{1-\nu} \tag{7.5-13}$$

and equals 1.6 for ν=0.22.

According to this the sensitivity is highest if the strain gauge is placed near the clamping of the cantilever. When considering also that the bi-axial bending of the beam (ε_x=ε_y) makes the cantilever stiffer through the bi-axial modulus $E/(1-\nu)$ compared to the plate modulus $E/(1-\nu^2)$ near the clamp, the effective sensitivity for the clamped resistor is even better than that for the un-clamped:

$$\text{A}: \frac{\Delta R}{R} = \frac{4\nu\varepsilon_x}{1-\nu} \text{ and } \varepsilon_x \propto (1-\nu) \Rightarrow \frac{\Delta R}{R} \propto 4\nu \quad (7.5\text{-}14)$$

$$\text{B}: \frac{\Delta R}{R} = \frac{(1+\nu)\varepsilon_x}{1-\nu} \text{ and } \varepsilon_x \propto (1-\nu^2) \Rightarrow \frac{\Delta R}{R} \propto (1+\nu)^2 \quad (7.5\text{-}15)$$

making the sensitivity difference close to a factor of 2 in favor of the clamped resistor.

So in order to achieve maximum sensitivity, the strain gauge should be placed close to the clamping of the cantilever.

7.5.2 Expected sensitivity and resolution

The above found gauge factors can now be used to estimate the sensitivity and resolution of the cantilever sensor with respect to surface stress.

The realised cantilevers have a length of 200 µm. The two SU-8 layers have a thickness of 4.5 µm and 1.7 µm. The gold resistor in between has a thickness of 400 Å and covers about 2/3 of the cantilever and an adhesion layer of 20 Å of titanium is used. The obtainable sensitivity and resolution with regard to surface stress have been calculated and the results listed in table 7.1. The gold resistor structure consists of a 5 µm wide meander structure with 14 turns of length 200 µm summing up to 310 Ω. It is assumed that only Johnson noise contributes

k [N/m]	f [kHz]	$\sigma_{s\ min}$ [N/m]	$\frac{\Delta R}{R}\sigma_s^{-1}$ [(N/m)$^{-1}$]
3.2	51	$9.8 \cdot 10^{-4}$	$6.5 \cdot 10^{-5}$

Table 7.1: Expected performance for the realised SU-8 cantilevers. Data used: t_{SU-8}: 4.5 µm and 1.7 µm, K=1.1, L=205 µm, w=100 µm, λ=200 µm, V_{in}=1 V, E_{SU-8}=4.4 GPa, ν=0.22, E_{gold}=79 GPa, $E_{titanium}$=116 GPa and Δf:1-51 Hz. The effective width and the effective Young's modulus of the metal layers are found by scaling with 2/3, *i.e.* w_{metal}=67 µm, $E_{gold\ resistor}$=53 GPa and $E_{titanium}$=77 GPa.

i.e. that 1/f noise is negligible as reported by Thaysen *et al.*[103]. The relatively low sensitivity compared to the silicon sensors is compensated by a low noise level and the resolution is comparable to that of the polysilicon sensors.

Potential resolution with new design

If the new design rule found above is followed, so that the strain gauge is placed near the clamping, an estimate of the potential for the SU-8 cantilevers as surface stress sensors can be given. The results for a cantilever with width and length of 200 µm and a strain gauge length of 100 µm are given in table 7.2. A resistance of 310 Ω is again assumed for the strain gauge. The resistor still has a thickness of 400 Å but the two SU-8 layers are assumed to have thicknesses of 1 and 3 µm. Compared to the expected performance calculated for the realised cantilevers,

k [N/m]	f [kHz]	$\sigma_{s\ min}$ [N/m]	$\frac{\Delta R}{R}\sigma_s^{-1}$ [(N/m)$^{-1}$]
1.6	31	$3.6 \cdot 10^{-4}$	$1.8 \cdot 10^{-4}$

Table 7.2: Expected performance for SU-8 cantilevers with strain gauge placed near clamping. Data used: t_{SU-8}: 3 µm and 1 µm, K=1.6, L=200 µm, w=200 µm, λ=100 µm, V_{in}=1 V, E_{SU-8}=4.4 GPa, ν=0.22, E_{gold}=79 GPa, $E_{titanium}$=116 GPa and Δf:1-51 Hz.

the gauge factor is $(1+\nu)/(1-\nu)$ instead of $4\nu/(1-\nu)$ and the plate modulus is used instead of the bi-axial modulus.

As seen in chapter 3 this solution can only be approximate as a numerical solution is needed to get a precise estimate of the strain in the cantilever near the clamping.

According to these numbers the SU-8 cantilever with metal strain gauge has the potential to surpass the polysilicon sensor as it has a comparable sensitivity and a presumably much lower inherent noise.

7.6 Summary

So far few working chips have been made, mainly due to problems with adhesion and with making electrical contact to the chip. Therefore no biochemical tests have been done yet.

It was shown that the SU-8 cantilever sensor has the potential of achieving a higher resolution than that of the polysilicon sensor. At the same time the processing time is shorter and the costs are lower for making the SU-8 sensor compared to the conventional silicon sensor.

A new design rule for designing the cantilever with metal strain gauges for optimised sensitivity with respect to in-plane stresses was calculated.

Chapter 8

Conclusions

The main goals of this Ph.D. work were to

- Optimise the sensitivity to surface stress for cantilever sensors with integrated readout.

- Make a cantilever sensor with integrated readout that can operate in liquids.

Analytical expressions for the sensitivity as a function of isotropic in-plane stress were derived. These showed how the sensitivity of a piezoresistor critically depends on its placement on the cantilever, not because of the stress concentration resulting from the concentrated force found in AFM, but because of the influence from the clamp on the strain distribution. These findings were specifically utilised in the design of both cantilever sensors with single crystalline silicon piezoresistors and cantilever sensors with integrated metal strain gauges. In both cases the result was a new design rule scheme for the surface stress sensors.

Using the new design rule scheme it was demonstrated that for the single crystalline silicon resistor in a cantilever(on (100) silicon with resistors placed along the [110] direction), where both strains along the length and the width of the resistor are present, n-type silicon will make the best choice as the piezoresistor.

For the polymer cantilever with an integrated metal strain gauge it would be expected that the highest sensitivity is obtained by placing the strain gauge close to the clamp of the cantilever, which is caused by two effects: (1) the constriction along the width of the cantilever makes the pure geometrical resistance change largest here and (2) on the cantilever, where the clamp is not felt, the isotropic stress will bend the cantilever both along its length axis and along its width axis, which effectively makes the cantilever stiffer.

Three different types of cantilever sensors, two of which are mentioned above, were designed and made during the project:

- Sensors with polysilicon piezoresistors and titanium silicide wiring.
- Sensors with single crystalline silicon piezoresistors.
- Sensors of SU-8 with gold strain gauges.

For the **polysilicon** sensor, the wiring of titanium silicide and the piezoresistors were encapsulated in LPCVD silicon nitride. It was found that the boron doped silicon and the titanium silicide had a high specific contact resistance, which made it necessary to make the resistors and the wiring of two different silicon layers with a large interface area. Additionally, incompatibility of silicon nitride and titanium silicide, with respect to thermal expansion coefficients, made annealing at high temperatures of this material combination impossible. It was also found that the silicon resistors annealed at high temperature in a furnace had a much lower 1/f noise than resistors annealed with an RTA process. The combination of these two problems made it necessary to form and anneal the piezoresistors prior to making the silicide wiring. The resulting sensors had resistors and wiring fully encapsulated in LPCVD silicon nitride and the interface contact between silicon and silicide had a contact resistance which is negligible compared to that of the total resistance.

A new piezoresistive sensor on an SOI substrate was presented. This sensor features a **single crystalline** silicon piezoresistor encapsulated in LPCVD silicon nitride. Tests indicated that this first generation was not efficiently encapsulated, but it is considered likely that a new mask set will be able to solve this problem. An estimate of the resolution that is obtainable with an optimised SOI sensor design was given, and it is only a factor of three lower than the measurement limit set by the thermal vibration noise.

An all-**SU-8** device with cantilevers integrated in a liquid channel was presented. Problems with metal adhesion to the SU-8 still remains to be solved, but the SU-8 sensor promises a resolution even better than that of the cantilever with polysilicon piezoresistors, though the readout is made with a gold strain gauge.

Due to the advantages presented by new approaches to cantilever design, I am confident that some of the aspects of the presented work will be implemented in new cantilever based biochemical sensors. The titanium silicide wiring and silicon nitride coating scheme represents a wafer scale, micromachining approach for making shielded wiring on any device, where electrical wiring close to the analysed reagents is necessary. The SOI sensor needs further development but promises a very high resolution. The SU-8 platform, on the other hand, aims at another niche where price per component, and not maximum resolution, is the main driver.

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Appendix A

Publications and conference contributions

P.A. Rasmussen, J. Thaysen, O. Hansen, S.C. Eriksen, and A. Boisen. Cantilever Biosensor with Integrated Read-out Optimised for Operation in Liquid. *The 16th European Conference on Solid-State Transducers, Proceedings*, pp 1202–1204, 2002.

P.A. Rasmussen, J. Thaysen, S.C. Eriksen, and A. Boisen. Optimised cantilever biosensor with piezoresistive read-out. *Presensted at Scanning Probe Microscopy, Sensors and Nanostructures, Las Vegas 2002.*

P.A. Rasmussen, J. Thaysen, O. Hansen, S.C. Eriksen, and A. Boisen. Optimised cantilever biosensor with piezoresistive read-out. *Ultramicroscopy*, 97(1-4):371–376, 2003.

M. Calleja, P.A. Rasmussen, A. Johansson, and A. Boisen. Polymeric mechanical sensors with piezoresistive readout integrated in a microfluidic system. *Proceedings of the SPIE - The International Society for Optical Engineering*, 5116:314–21, 2003.

M. Calleja, P. Rasmussen, A. Johansson, and A. Boisen. Polymeric mechanical sensors with strain gauge readout in a microfluidic system. *Accepted for μTAS, October 2003.*

A.V. Grigorov, Z. Davis, P. Rasmussen, and A. Boisen. A longitudinal thermal actuation principle for mass detection using a resonant microcantilever in a fluid medium. *Accepted for MNE, September 2003.*

M. Calleja, J. Tamayo, A. Johansson, P. Rasmussen, L. Lechuga, and A. Boisen. Polymeric cantilever arrays for biosensing applications. *Accepted for Sensors Letters.*

Appendix B

Process sequence, 1st generation polysilicon sensor

1 Deposit sirich silicon nitride, 50.5 min, 835 °C, ∼2100 Å

2 Deposit poly silicon, TAMORPH 580 °C, 49 min, ∼2200 Å

3 **Mask wires**. Bake resist on hotplate for 90 s@120 °C (or 25 min@120 °C, furnace).

4 Etch with poly-etch to define electric interconnections.

5 Strip resist.

6 **Mask silicide**

7 Dip in BHF for 20 s, deposit 800 Å of titanium.

8 Pattern titanium by lift-off

9 RTA at 850 °C for 60 s using thermo-couple. 10 min with Ar-flow with wafer in chamber before anneal. Etch remaining titanium in piranha (H_2SO_4:H_2O_2 4:1) for 10 min.

10 Deposit microcrystalline silicon, POLY620, 15 min (620 °C, 80 sccm SiH_4 0 0, 250 mTorr), 1600 Å. (no RCA - destroys silicide) [three test wafers]

11 Boron implantation: $3.7{\cdot}10^{15}$ cm^{-2} at 30 keV [three test wafers]

12 **Mask implant**

13 Boron implantation: X $(3.7/7.4){\cdot}10^{15}$ cm^{-2} at 30 keV

14 Strip mask with acetone. Perhaps oxygen plasma.

15 Mask resistors

16 Etch in RIE with AB_ANISO to define resistors. Endpoint when reaching silicon nitride.

17 Strip resist. Piranha

18 Deposit sirich silicon nitride, 12 min, 835 °C, ∼500 Å. [three test wafers]

19 Anneal RTA at 900 °C (mindst) for 60 s (TC). [three test wafers]

20 Mask probe

21 RIE (AB_ANISO) both nitride layers. Endpoint when reaching silicon substrate.

22 Strip resist

23 Mask metal_cantilevers(or _left, _right)

24 Deposit metal. Lift-off

25 Mask pads(or pads_ledebaner for electrical contact to metal)

26 Deposit metal. Lift-off

27 Anneal metal/silicide contact?

28 Mask bagside

29 RIE back (Si_3N_4/Si/Si_3N_4 1900 Å/1400 Å/500 Å), AB_ANISO [front protection?]

30 Etch from back in KOH with front protection.

- end of process sequence

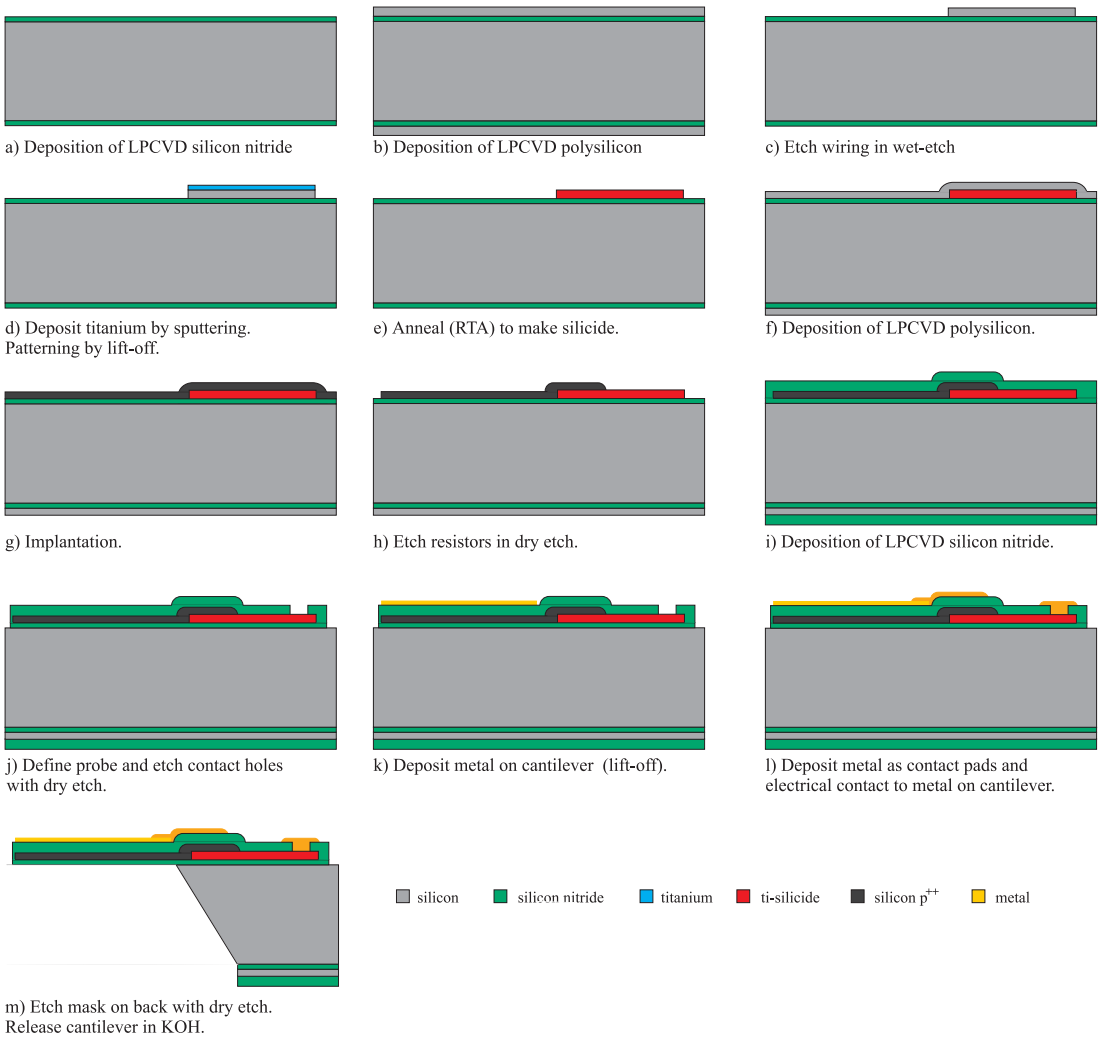


Figure 2.1: Process sequence.

Appendix C

Masks, 2nd generation polysilicon sensor

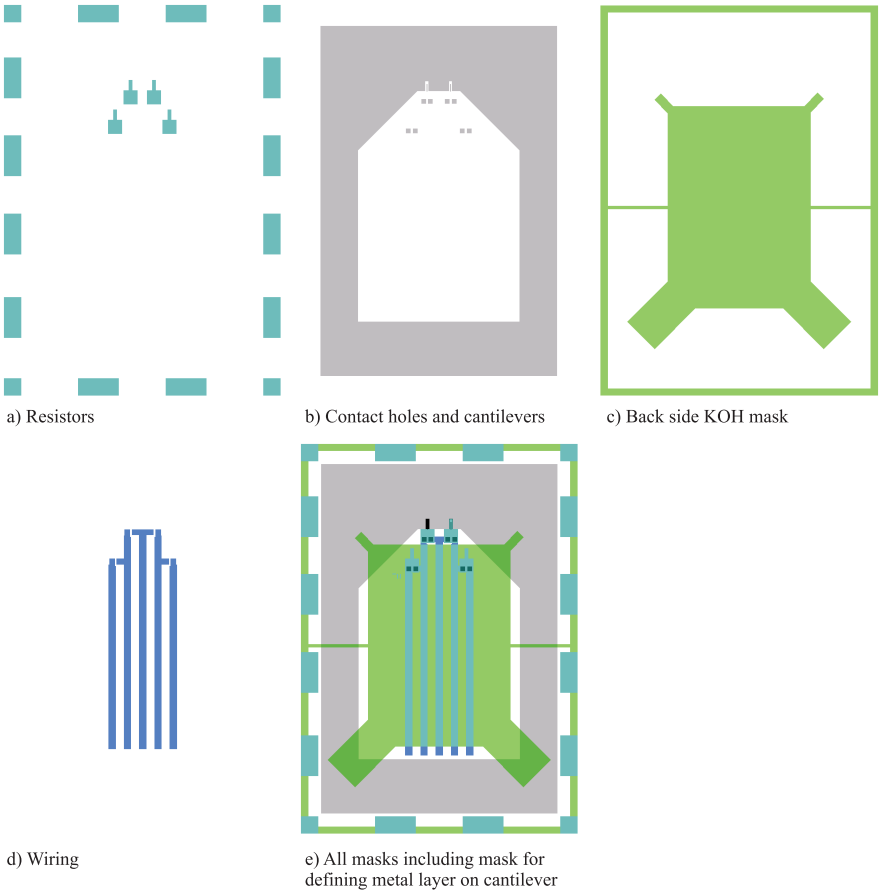


Figure 3.1: Mask set for the 2nd generation polysilicon sensor.

Appendix D

Process sequence, 2nd generation polysilicon sensor

Chips with gold wiring

Alle masker på nær 'bagside' skal på forsiden af skiven, dvs. den side, der implanteres.
Alle masker defineres i 1.5 μm resist, belyses ca. 9 s i KS eller ca. 7 s i EVC. Fremkaldes ca. 60-65 s.(standard) Benyt 'contact mode' på alignere.
På plastikboksene med masker i er navngivningen 'FP RESISTOR', 'FP NITRID', ... Navn i parentes i procesfølgen er det navn, Delta Mask har skrevet på selve masken.

6 dobbeltsidepolerede skiver (ON63)

1 Deposit sirich silicon nitride, 50.5 min, 835 °C, 2100 Å. Sirich (93 DCS, 13 NH_3). To testskiver med. En til at måle tykkelse af nitrid på ellipsometer og en til måling af polylag i step 2.
Tykkelse målt på ellipsometer: *2218 Å.*

2 Deposit poly silicon, POLY620 14 min (1470 Å)
Tykkelse målt på tencor efter æts i polyæts med blå film: *ca. 1500 Å.*

3 Implant boron, 30 keV, $4.4 \cdot 10^{15}$ cm^{-2}.

4 Clean with 7-up.

5 **Mask Resistor** ('Nitride') Align til flat. Brug EVC-aligner til første belysning for at få god aligning til flat. Benyt 'hard contact mode'.
Denne maske definerer siliciummodstande på bjælkerne.

6 RIE1, AB_ANISO (som OH_POLY): endpoint when reaching nitride; approx. 1 min (incl. 20 s overetch). Endpoint falder, når nitrid nås. Kant- og bagsidebeskytter.

7 Strip resist = acetone.

7B **NB** For de tre skiver uden nitrid på. Resist spinnes på forsiden, bages 120 °C f.eks. med REV100s på Track1 eller 2.
5 min i polyæts med N_2-bobbler.
Strip resist. (Fjerner poly på bagside, så RIE i step 18 bliver kortere.)

8 7-up

9 Deposit silicon nitride: 12 min SIRICH (93 DCS, 13 NH_3), 500 Å. Testskive med til tykkelsesmåling på ellipsometer.
Tykkelse ni:

10 Deposit TEOS (standardprocessen, flow 50, 30, 0, 0, temp. 725 °C). 35 min deponering (ca. 3500 Å). To testskiver med til tykkelsesmålinger. En skive tages direkte med over i annealovn.
Tykkelse TEOS:

11 Anneal 1100 °C, 20 min, flow 6 SSL N_2.
Tykkelse TEOS efter anneal:

12 **Mask Nitrid** ('Coat')
Denne maske definerer bjælken. Hele modstanden (ætset i step 6) på bjælken skal være indkapslet i nitrid, dvs. det er vigtigt at tjekke, at masken ligger lige. Modstanden må ikke 'stikke ud'.

13 Blå film på bagside af skive, så TEOS dækker nitrid i fosforsyren.
Ætsi BHF. 750 Å/min + 2 min ekstra. (Ex. 3500 Å ætses på 4.7 min dvs. 7 min dyp ialt.)

14 Strip resist = acetone.

15 Etch nitride in phosphoric acid, 180 °C, **120 min**. (2700 Å, $\text{etch}_{\text{min}} = 30$ Å/min $\longrightarrow$ 90 min). Én skive først. Evt. tjekke om kontakt i studenterrum.

16 Strip TEOS i BHF 10 min.

17 **Mask Bagside** ('Metal') På bagside af skive til friætsning af bjælker i KOH.

18 RIE bagside. Kantbeskytter
Hvis poly fjernet på bagside: 2700 Å ni - 12 min JT_NITR3.
Hvis stadig poly i mellem de to nitridlag: 4200 Å - 16 min JT_NITR3.

I første omgang glemmes nedenstående.
RIE1, back. (500 ni/1500 si/2100 ni)

90 s AB_ANISO: ca. 500 Å ni plus 1500 Å si. Bør kunne ses på endpoint, da endpoint vil falde, når si nås, og stige igen ved nederste nitridlag. AB_ANISO bør stoppes ved det nederste lag ellers blot ved 90 s. Fortsæt æts med JT_NITR3 9 min. Denne æts er en fysisk æts og vil derfor ikke i samme grad som AB_ANISO ætse på forsiden af skiven.
For både JT_NITR3 og AB_ANISO er ætseraten i nitrid ca. 400-500 Å/min. I silicium ætser JT_NITR3 ca. 400-500 Å/min mens AB_ANISO ætser ca. 3000 Å/min.
Overæts på bagsiden af skiven er ikke et problem her, da den senere skal ætses i KOH. Problemet her er at skåne nitriden på forsiden af skiven.

19 Strip resist = acetone.

20 **Mask Ledebaner** ('Backside') Denne maske definerer ledebaner på chippen.

21 (BHF dyp 20 s for at fjerne oxid.) Alcatel Cr/Au 100/2000 (Vedhæftningslag skal være krom, da skiven bliver udsat for KOH i sidste procestrin.)

22 Lift-off.

23 **Mask Au2** ('Cantilever') (Med krom op og tekst nede i højre hjørne vender masken op.)
Denne maske definerer et metallag på en af bjælkerne. Masken (hullet) skal derfor ligge indenfor omridset af bjælken. Ikke kritisk hvis maske lige rører 'kanten'.

24 Lad os aftale metalkombination. Der skal sandsynligvis ikke det samme på dem alle.
Alcatel Use plasma(in Alcatel): 100 W, 5 min before deposition. Metal e.g. Cr/Au/Ni 50/400/300. I samme deponering! Dvs. vacuum må ikke brydes, så alle tre metaller skal være i.

25 Lift-off

26 Etch from back in KOH with front protection. Ingen bobler i skyllekar når bjælker er ætset, ingen tørring i spin-dryer! Tør i luft eller spritfase.

- end of process sequence

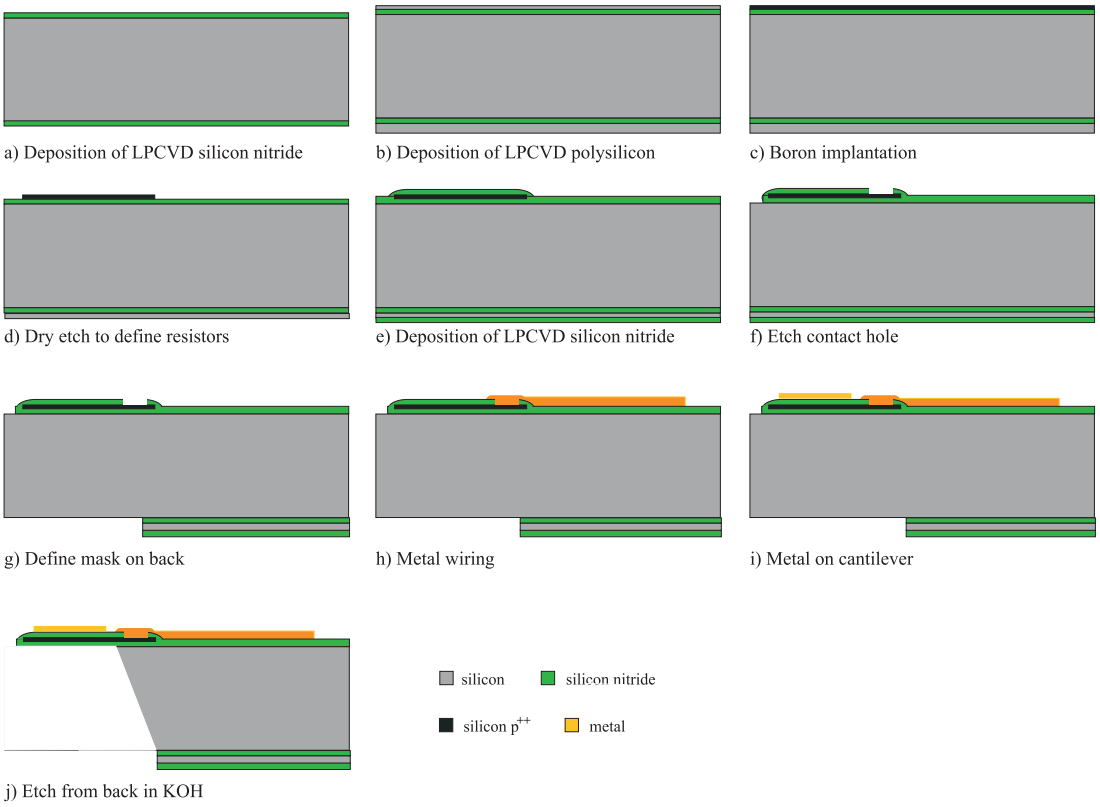


Figure 4.1: Process sequence

Process sequence, 2nd generation silicide wiring

1 Dep. 2100 Å sirich (44 min) (testskiver)
2 Dep. TAMORPH 2200 Å (49 min)
3 Au mask (negativ)
4 polyæts, strip resist
5 Au mask
6 BHF 20 s, dep. 800 Å ti
7 lift-off
8 RTA 850 °C / 60 s
9 piranha
10 Dep. POLY620 1470 Å
11 Implant B^{11}, 30 keV, $4.4 \cdot 10^{15}$ cm^{-2}
12 Cantilever mask
13 RIE, strip resist
14 piranha
Ex:
15 Dep. sirich 5 min
16 RTA 900 °C / 60 s
17 piranha
18 Dep. sirich 8 min
19 Nitride mask
20 RIE ab_aniso 2 min, strip resist
21 Back side mask
22 RIE back approx. 5 min with JT_NITR3 – overetch (=9 min total), strip resist
23 Au mask
24 BHF 20 s, dep. Cr/Au 150/3000
25 Lift-off
26 Au2 mask (cantilever)
27 Plasma clean, Cr/Au/Ni 50/400/300
28 Lift-off
29 KOH

Appendix E

Process sequence, 3rd generation polysilicon sensor

Double sided polished wafers (350 μm)
All mask steps (**bold** font) with 1.5 μm resist, hard contact mode on KS Aligner. HMDS before resist except if resist is spun onto gold as in some of the last steps. All masks on front of wafer (implanted side) except for the mask 'bagside'.

1. Deposit LPCVD silicon nitride: Sirich (93 DCS, 13 NH_3), 60 min (2500 Å)
   3 test wafers: 1 dummy, 1 for poly si thickness(step 2), 1 for ni thickness:

2. Deposit LPCVD polysilicon: POLY620, 14 min (1500 Å)
   Test wafer, thickness si:

3. Boron implantation: $3.5 \cdot 10^{15}$ cm^{-2}, 30 keV ($2.3 \cdot 10^{20}$ cm^{-3})
   Scriber top, front of wafer: 1, 2, ...

4. Piranha/7-up. Deposit LPCVD silicon nitride: Sirich (93 DCS, 13 NH_3), 5 min (200 Å, precise thickness not important)

5. Anneal 30 min at 1100 °C (N_2-flow)

6. Strip nitride in phosphoric acid (180 °C), 10 min

7. Check surface resistance to check if nitride is totally removed (*4 pp if possible else 2 pp to check if contact, PRA*)

8. **Mask: resistors**

9. RIE resistors, AB_ANISO on RIE1 (if using RIE2 use OH_POLY or similar standard anisotropic silicon etch: 40 SF_6, 8 O_2, 30 W, 80 mTorr), ~30 s. Follow endpoint signal and abort manually. Endpoint signal goes **up** when reaching nitride layer, wait till endpoint signal levels again (~20 s over etch)

10. Strip resist in acetone

11. Piranha: H_2SO_4:H_2O_2 approx. 1000 ml:200 ml in glass beaker for 10 min.

12. Deposit LPCVD silicon nitride: Sirich (93 DCS, 13 NH_3), 10 min (400 Å)
    Test wafer, thickness ni: (test wafer to step 18)

13. Mask: CRE nII

14. RIE1: JT_NITR3, 2 min. *Check resistance on first wafer to check if nitride removed (PRA).*
15. Check resistance (PRA)

16. Strip resist in acetone

17. Piranha/7-up (+test wafer from step 12)

18. Deposit LPCVD poly silicon: TAMORPH, 55 min (~2500 Å) (+test wafer from step 12)

19. Mask: wiring

20. RIE wiring, AB_ANISO on RIE1, ~60 s otherwise follow endpoint signal as step 9.
(+above test wafer; no mask on test wafer)

21. Strip resist in acetone

22. Mask: silicide

23. Plasma: asher 200 W 120/20/0 2 min, BHF 15 s, deposit 800 Å Ti

24. Lift-off

25. RTA 725 ℃ / 60 s (pyro), 15 min Ar-flow (PRA)

26. Check resistance (PRA)

27. Piranha, as step 11 (to remove titanium)

28. Deposit LPCVD silicon nitride: Sirich (93 DCS, 13 NH_3), 12 min (500 Å)
[7-900 Å ni in total on top] Testwafer+Testwafer from step 20
$ni_{step\ 28}$: $ni_{step\ 12+step\ 20+step\ 28}$:

29. Mask: probe nII

30. RIE: AB_ANISO on RIE1, ~10 min. Etching through approximately 3300 Å silicon nitride and the etch rate is usually 300-400 Å/min. Endpoint will **fall** when the nitride layer has been etched and the silicon substrate is reached. Use holder+edge protection.

31. Strip resist in acetone

32. Mask: CLB nII

33. RIE: AB_ANISO on RIE1, 3 min. *Check resistance on first wafer(PRA)*

34. Strip resist in acetone

35. HMDS, spin resist on front (PR1_5)

36. Spin resist (1.5_NB) on back, bake in 90 °C furnace 25 min

37. Mask: bagside (rear side alignment)

38. RIE mask on rear side: AB_ANISO on RIE1, ~12 min, endpoint **falls** when reaching silicon substrate

39. Strip resist in acetone

40. Mask: pads

41. Plasma 120/20/0 200 W 2 min. Deposit Cr/Au 50/1000 in Alcatel

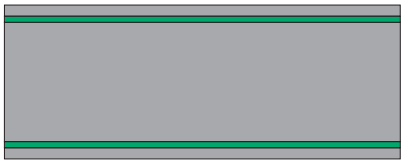
42. Lift-off

43. Mask: metal_cantilever (most likely mask for metal deposition on left cantilever)

44. Plasma. Deposit Cr/Au 50/400 in Alcatel

45. Etch in KOH with front side protection ~4.5 h

a) Deposition of LPCVD silicon nitride

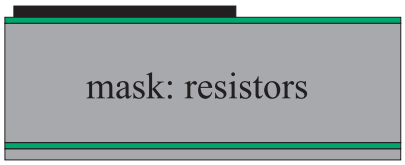


b) Deposition of LPCVD polysilicon

c) Boron implantation

d) Deposition of LPCVD silicon nitride before anneal

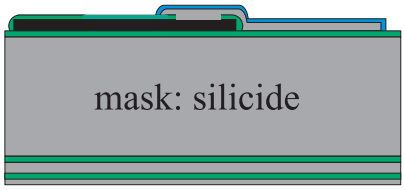
e) Strip of silicon nitride



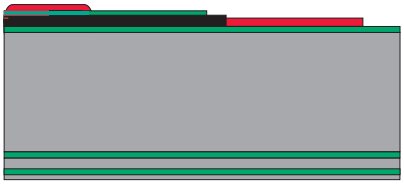
f) Etch resistors with RIE

g) Deposition of LPCVD silicon nitride and contact holes opened with RIE

h) Deposition of LPCVD polysilicon and patterning of wiring with RIE



i) Deposition of titanium patterned with lift-off

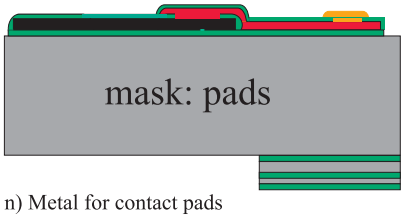


j) RTA to make silicide

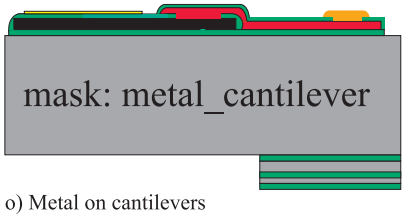
k) Deposition of LPCVD silicon nitride. Probe etched with RIE.

l) Contact holes opened with RIE.

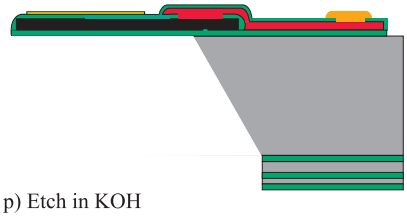
m) Mask on rear side defined with RIE



n) Metal for contact pads



o) Metal on cantilevers



p) Etch in KOH

Appendix F

Process sequences for silicon wiring

Implant

One sided polished wafers, low doped n-type (ON61)

1 Deposit 500 Å silicon nitride, recipe: sirich, 12 min (835 °C) (10 wafers)

2 Deposit 5000 Å poly, recipe: poly620 (-1 wafer; only resistors)

3 Boron implantation: $5{\cdot}10^{16}$ cm^{-2}, 50 keV (2 skiver (implantering tager lang tid!))

4 **Mask wiring**, 1.5 μm resist

5 Etch in poly-etch or RIE

6 Deposit 1600 Å silicon, poly620, 15 min

7 Boron implantation: $3.2{\cdot}10^{15}$ cm^{-2}, 30 keV

8 **Mask resistor**, 1.5 μm resist

9 RIE, ab_aniso (endpoint when reaching silicon nitride)

10 Deposit 500 Å silicon nitride, recipe: sirich, 12 min (835 °C)

11 #1: KOH, 30 min, 80°C
#2-3: anneal 1000°C/20 min + KOH
#4-5: anneal 1000°C/1 min (RTA) + KOH

12 probe mask+RIE: measure resistance+test structures(metal) (e.g. 1,2,4)
strip nitride(phosphoric acid): measure resistance wiring/resistor (e.g. 3,5)

In situ wiring I

5 one sided polished wafers, low doped n-type (ON61)

1 Deposit 500 Å silicon nitride, recipe: sirich, 12 min (835 °C)

2 Deposit ∼1 μm poly si, recipe: TMIC580, 4 h, SiH_4: 80, B_2H_6: 7

3 **Mask au** HMDS, 1.5 μm resist(KSF spinner: coating+baking/MIC1_5_4"+90C_60s, rens: kun 'coating' clean_chuck_w_wafer), KS-aligner: 7 s - bake Rev100s on track1 (120 °C) - flood exposure 25 s (lamp test) - development

4 Etch of wiring

Test one wafer in polyœts(hard bake resist before: Rev100s); if etch doesn't work then wiring is etched with RIE (∼2-3 min)

5 Strip resist in acetone(1 min grov, 6 min fin); check with microscope - if resist is not totally removed then plasma asher(500 W, 10 min, 210 O_2 (recipe 6); CF4!)

5 Check resistivity; measure resistance with two-point probe if possible.

In situ wiring I

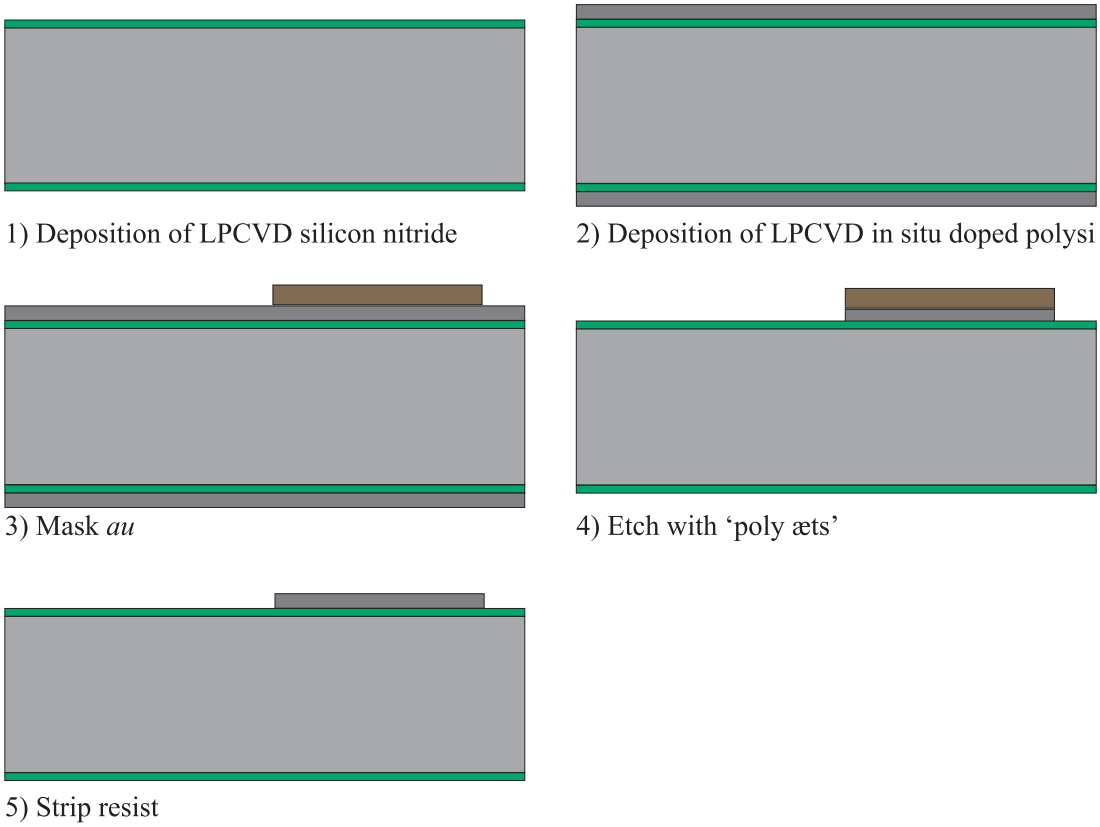


Figure 6.1: Process sequence in situ.

In situ wiring II

6 Clean wafers: RCA.

7 With wafers #1-2: Deposit 500 Å silicon nitride, recipe: sirich, 12 min (835 °C)

8 With wafers #3-5: Deposit silicon, recipe: POLY620, 1600 Å

9 #1: RTA 1000 °C, 60 s

10 #1-2: strip nitride in phosphoric acid, 17 min. Measure resistance.

Wafer	R_1	R_2	R_3	R_4	$\overline{R}$	ρ
#1 (RTA)						
#2						

Measure on wires on the outermost left/right

11 #3-5: Boron implantation: $3.2{\cdot}10^{15}$ cm^{-2}, 30 keV

12 #3-5: **Mask resistor** (not 'nychip' mask) HMDS, 1.5 μm resist

13 #3-5: RIE (RIE1) to define resistors (approx. 1 min)

14 #3-5: Strip resist in acetone. Clean wafers with piranha.

15 #3-5: Deposit 500 Å silicon nitride, recipe: sirich, 12 min (835 °C)

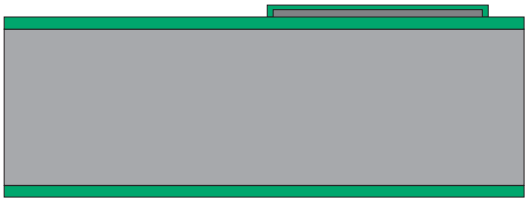
16 #4: Furnace anneal 1000 °C, 20 min

17 #5: RTA 1000 °C, 60 s

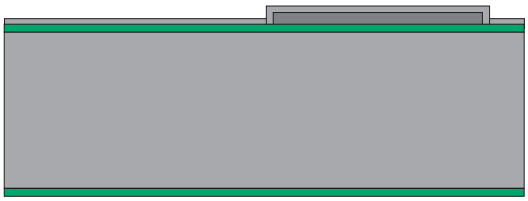
18 #3-5: Etch test KOH 80 °C, 30 min

19 #3-5: Clean wafers in 7-up. Strip nitride in phosphoric acid 17 min. Measure resistance, see page 142.

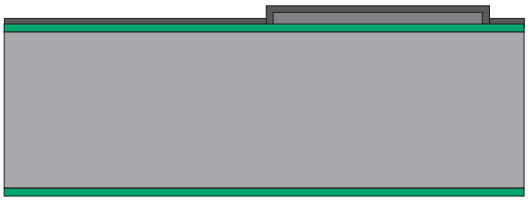
In situ wiring II



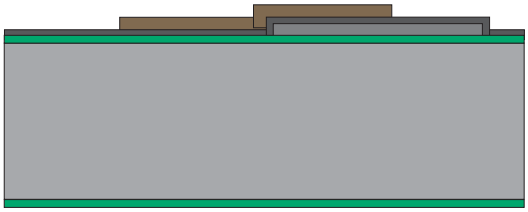
7) #1-2: Deposition of LPCVD si nitride



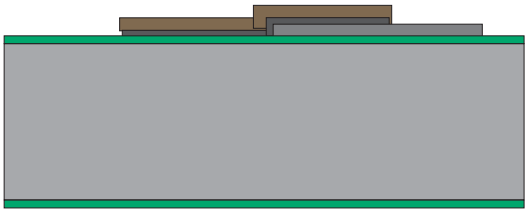
8) #3-5: Deposition of LPCVD polysilicon



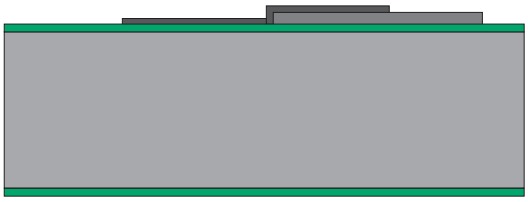
11) #3-5: Boron implantation



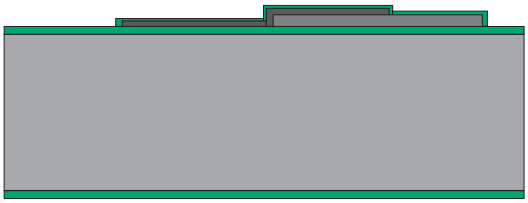
12) #3-5: Mask resistor



13) #3-5: RIE to define resistors



14) #3-5: Strip resist



15) #3-5: Deposit LPCVD si nitride

Figure 6.2: Process sequence in situ.

In situ wiring

Wiring:

Wafer	R_1	R_2	R_3	R_4	$\overline{R}$	ρ
#3 #4 Furnace #5 (RTA)						

Measure on wires on the outermost left/right

Wiring+resistor:

Wafer	25	50	66	87	132
#3 #3 #4 Furnace #4 Furnace #5 (RTA) #5 (RTA)					

Predep wiring I

10 one sided polished wafers, low doped n-type (ON61)

1 Grow 1 μm wet oxide, 110 min, 1150 °C

2 **Mask au** HMDS, 1.5 μm resist, KS-aligner: 10.5 s - develop

3 Post bake resist: Rev100s

4 Etch in BHF (next to spin dryer) approx. 15 min (750 Å/min)(si hydrophobic) Protect back of wafer.

Mark wafers with scriber; p1-10

5 Strip resist in acetone (1 min grov, 6 min fin)

6 RCA (cleaning of wafers before next furnace process). (+2 dummy wafers)

7 Bor predep furnace, recipe: BP1125, 3 h. Check one wafer in konc. HF (60 min, next to RCA bench, glass hydrophilic), other wafers on stand-by in furnace

8 Check resistivity; measure resistance with two-point probe. Measure on the outermost left/right.

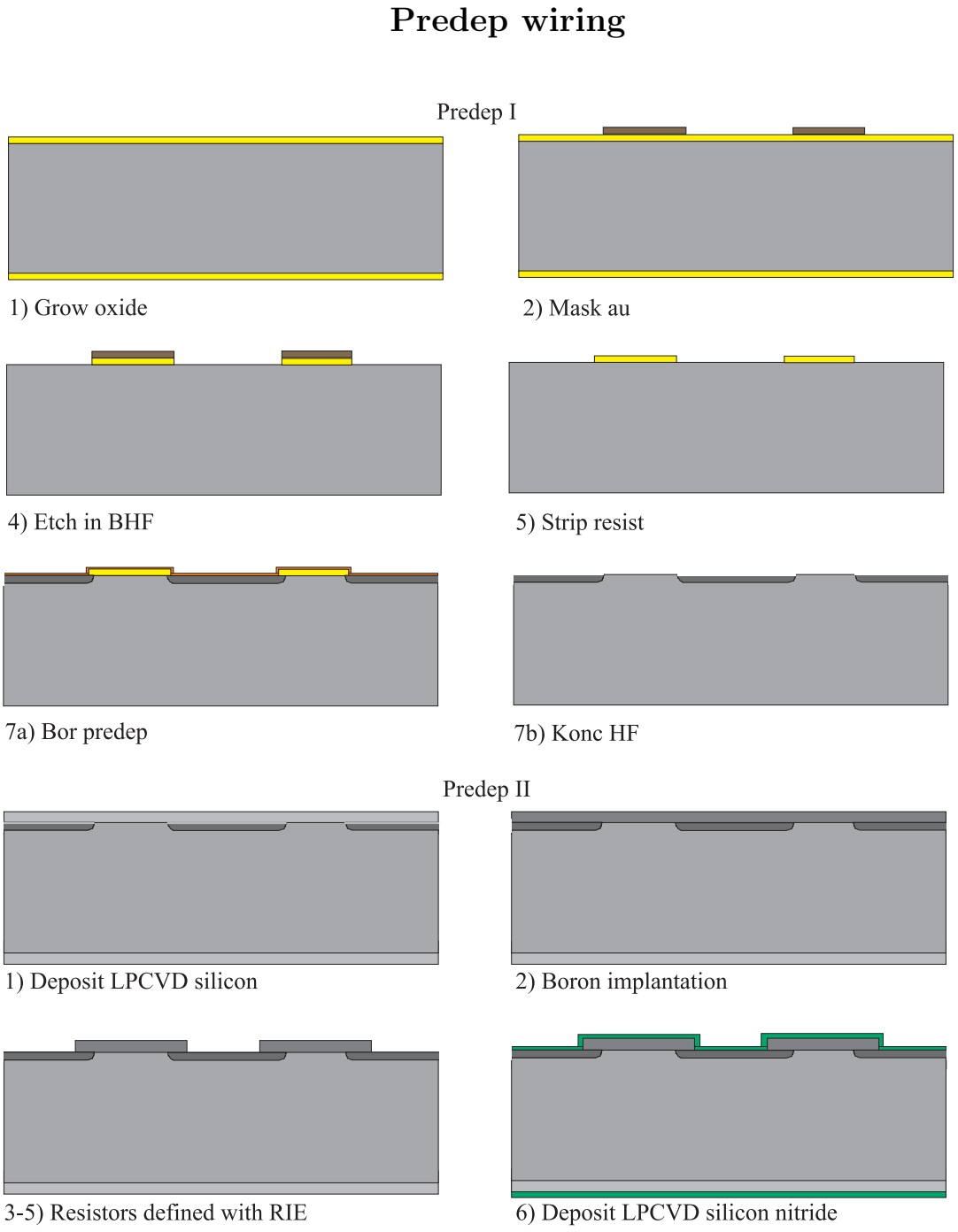


Figure 6.3: Process sequence predep.

Predep wiring II

5 wafers with (pre dep) implanted wiring

1 Clean wafers: RCA. Deposit silicon, recipe: POLY620, 1600 Å

2 Boron implantation: $3.2{\cdot}10^{15}$ cm^{-2}, 30 keV

3 **Mask resistor** (not 'nychip' mask) HMDS, 1.5 μm resist

4 RIE (RIE1) to define resistors (approx. 1 min)

5 Strip resist in acetone. Clean wafers with piranha.

6 Deposit 500 Å silicon nitride, recipe: sirich, 12 min (835 °C)

7 With wafer #1: Etch test KOH 80 °C, 30 min. Clean wafer in 7-up. Strip nitride in phosphoric acid 17 min. Measure resistance wiring/resistors (Table page 146). (If working continue with other wafers)

8 With wafer #2-3: Furnace anneal 1000 °C, 20 min

9 With wafer #4-5: RTA 1000 °C, 60 s

10 With wafer #2+4: Etch test KOH 80 °C, 30 min

11 With wafer #2+4: Clean wafers in 7-up. Strip nitride in phosphoric acid 17 min. Measure resistance, see table page 146.

Predep wiring

Wiring:

Wafer	R_1	R_2	R_3	R_4	$\overline{R}$	ρ
#1						
#2 Furnace						
#3 Furnace	-	-	-	-		
#4 (RTA)						
#5 (RTA)	-	-	-	-		

Measure on wires on the outermost left/right

Wiring+resistor:

Wafer	25	50	66	87	132
#1					
#1					
#2 Furnace					
#2 Furnace					
#3 Furnace	-	-	-	-	-
#3 Furnace	-	-	-	-	-
#4 (RTA)					
#4 (RTA)					
#5 (RTA)	-	-	-	-	-
#5 (RTA)	-	-	-	-	-

Appendix G

Process sequences I and II, SOI sensor

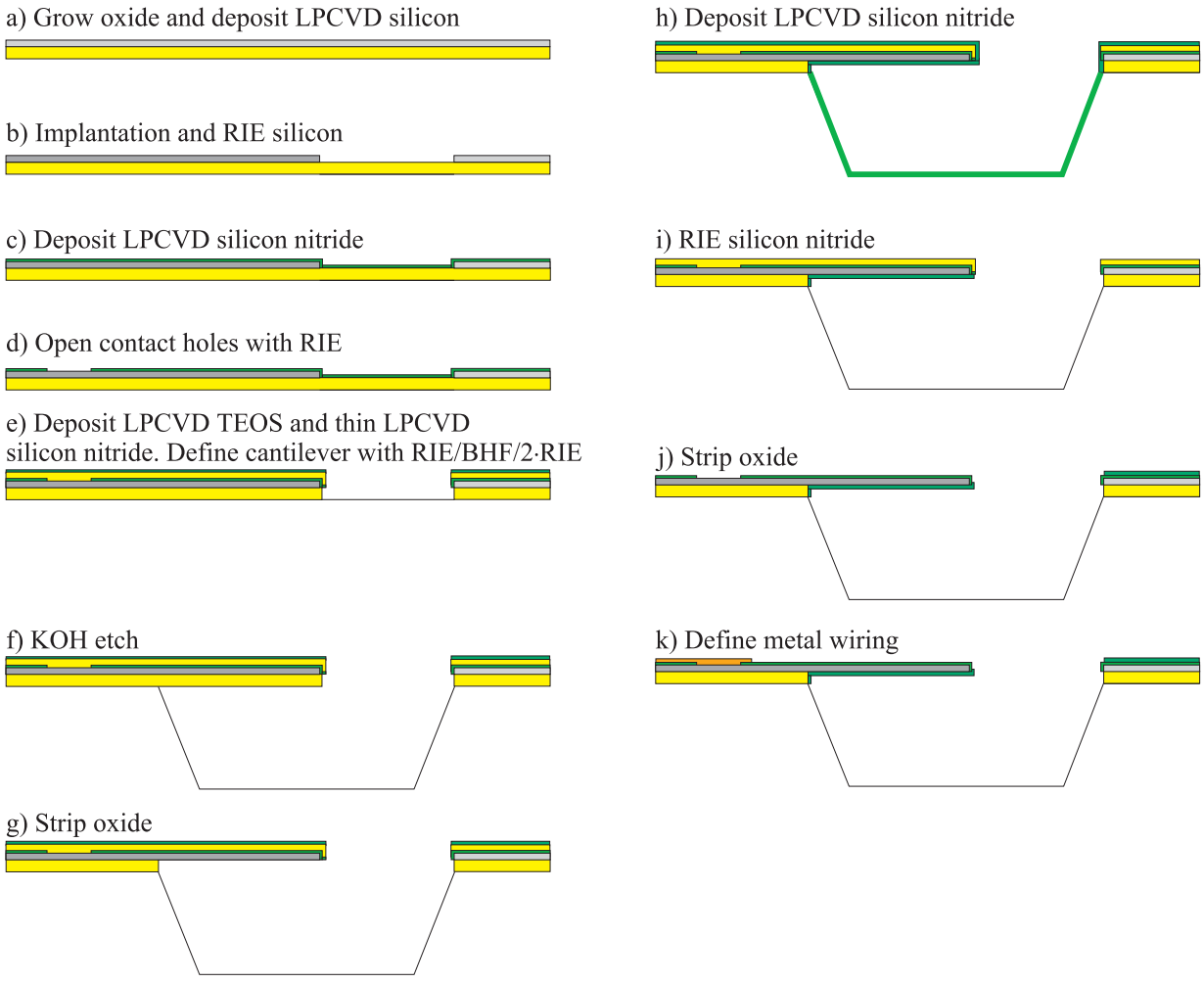
Process sequence I, SOI

single side polished wafers+soi
Test of 'front' process, masks: soichip and DNA_chip(jt)

1. 4000 Å wet oxide
2. 2200 Å poly (fig. a)
3. Implant $6.6 \cdot 10^{14}$ P, 40 keV
4. 7-up
5. **Mask 1**: resistor_soi
6. RIE poly
7. Strip resist (fig. b)
8. **Mask 2**: implant
9. Implant $6.6 \cdot 10^{15}$ P, 40 keV
10. Strip resist, acetone+plasma
11. Piranha + deposit 500 Å LPCVD ni (11 min) (fig. c) (Test wafer:)
12. **Mask 3**: kontakthuller_soi (neg AZ process)
13. RIE nitrid 500 Å, jt_nitr4 90 s.
14. Strip resist (fig. d)
15. Piranha + dep. 2000 Å TEOS (Test wafer:)
16. +anneal 1000 °C 20 min (Test wafer:)
17. +dep 100 Å sirich (3 min) (Test wafer:)
18. **Mask 4**: cant&kanal_soi
19. RIE ni jt_nitr4 1 min (100 Å)
20. BHF TEOS 4 min (2000 Å)
21. RIE ni jt_nitr4 90 s (500 Å)
22. RIE oxid pra_sio2 (360 Å/min) 15 min (4000 Å)
23. Strip resist (fig. e)
24. KOH 40 min (fig. f) (udbøjning:)
25. Strip oxid BHF 7 min (fig. g) (udbøjning:)
26. piranha
27. Dep 1000 Å sirich (22 min) (fig. h) (udbøjning:)
28. RIE jt_nitr3 4 min (1000 Å) (fig. i) (udbøjning:)
    RIE stop på oxid?
29. BHF 3 min. Strip TEOS oxide on top of cantilever (fig. j)

30. Metal dep Ti/Au 50/2000
31. **Mask 5**: metal_soi (neg AZ process)
32. Etch au
33. Etch ti; BHF dip
34. Strip resist (no ultrasonic aggitation)

(fig.k)



Process sequence II, SOI

single side polished wafers+soi
Test of 'front' process, masks: soichip and DNA_chip(jt)

1. 4000 Å wet oxide
2. 2200 Å poly (fig. a)
3. Implant $6.6 \cdot 10^{14}$ P, 40 keV
4. 7-up
5. **Mask 1**: resistor_soi
6. RIE poly+oxid: aniso ~1 min+ pra_sio2 15 min
7. Strip resist (fig. b)
8. **Mask 2**: implant 2.2 μm
9. Implant $6.6 \cdot 10^{15}$ P, 40 keV
10. Strip resist, acetone+plasma
11. Piranha + deposit 1000 Å LPCVD ni (22 min) (fig. c) (Test wafer:)
12. **Mask 3**: kontakthuller_soi (neg AZ process)
13. RIE nitrid 1000 Å, jt_nitr4 (ikke nitr3!) 150 s
14. Strip resist (fig. d)
15. Piranha + dep. 4000 Å TEOS (40 min) (Test wafer:)
16. +anneal 1000 °C 20 min (Test wafer:)
17. ~~+dep 100 Å sirich (3 min)~~ skipped! (RIE in step 20) (Test wafer:)
18. **Mask 4**: cant&kanal_soi 2.2 μm resist
19. ~~RIE ni jt_nitr4 1 min (100 Å)~~
20. ~~BHF~~ RIE TEOS: pra_sio2 15 min (4000 Å)
21. RIE ni ab_aniso ~150 s (1000 Å) (endpoint?)
22. ~~RIE oxid pra_sio2 (360 Å/min) 15 min (4000 Å)~~
23. Strip resist (fig. e)
24. KOH 45 min (fig. f) (udbøjning:) **÷ bubbler!**
25. 7-up + HCl (?) (udbøjning:)
26. piranha
27. Dep 2000 Å sirich (44 min) (fig. g) (udbøjning:)
28. RIE jt_nitr3 6 min (2000 Å) (fig. h) (udbøjning:)
    RIE stop på oxid?
29. BHF 5 min. Strip TEOS oxide on top of cantilever (fig. i)

30. Metal dep Ti/Au 50/2000
31. **Mask 5**: metal_soi (neg AZ process)(SU-8? soi1: metal i kanaler nogle steder)
32. Etch au
33. Etch ti; BHF dip (fumehood cleanroom 2)
34. Strip resist (no ultrasonic aggitation) (fig. j) + piranha

a) Grow oxide and deposit LPCVD silicon

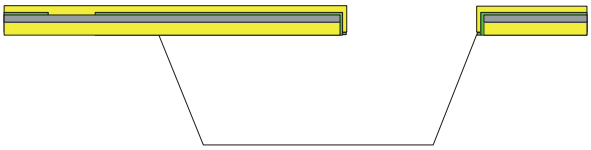
b) RIE silicon and oxide. Implantation

c) Deposit LPCVD silicon nitride

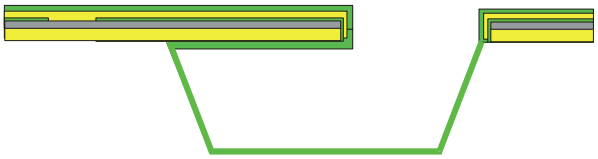
d) Open contact holes with RIE

e) Deposit LPCVD TEOS. Define cantilever with RIE

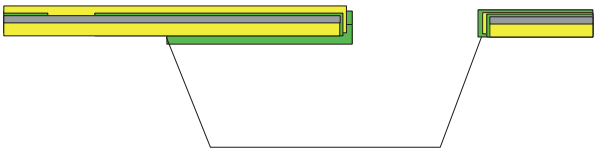
f) KOH etch



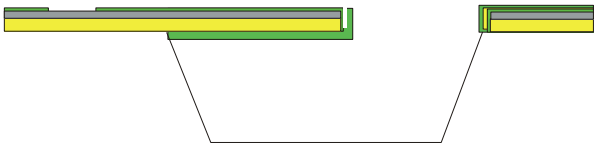
g) Deposit LPCVD silicon nitride



h) RIE silicon nitride



i) Strip oxide



j) Define metal wiring